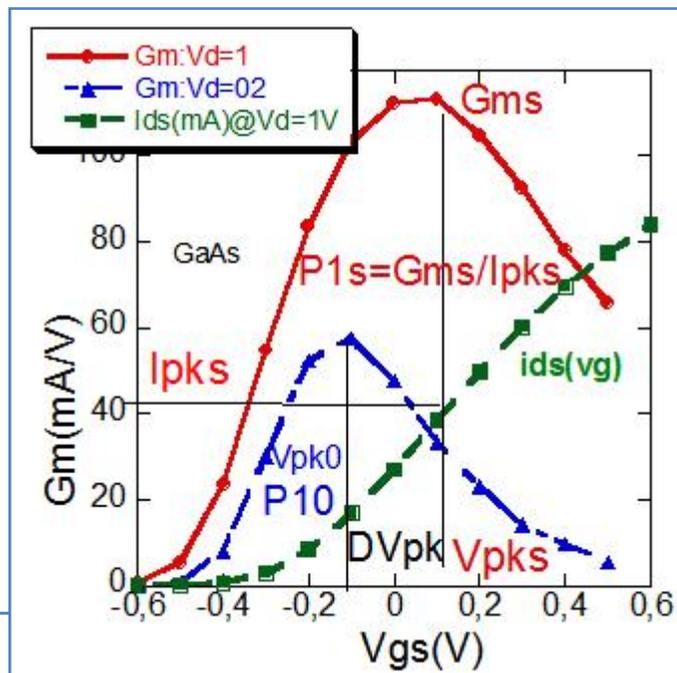


Angelov GaN Modeling

- Parameter Influence
- Parameter Extraction Strategy



sketch by courtesy of Prof. I. Angelov

Franz Sischka, Dec. 2020
www.SisConsult.de



Outline

- **Introduction to the Angelov Model**

- **Step-by-Step Modeling Sequence**

 - Resistances R_G , R_D , R_S

 - DC Input Characteristic i_g - v_{gs}

 - DC Transfer Characteristic i_d - v_{gs}

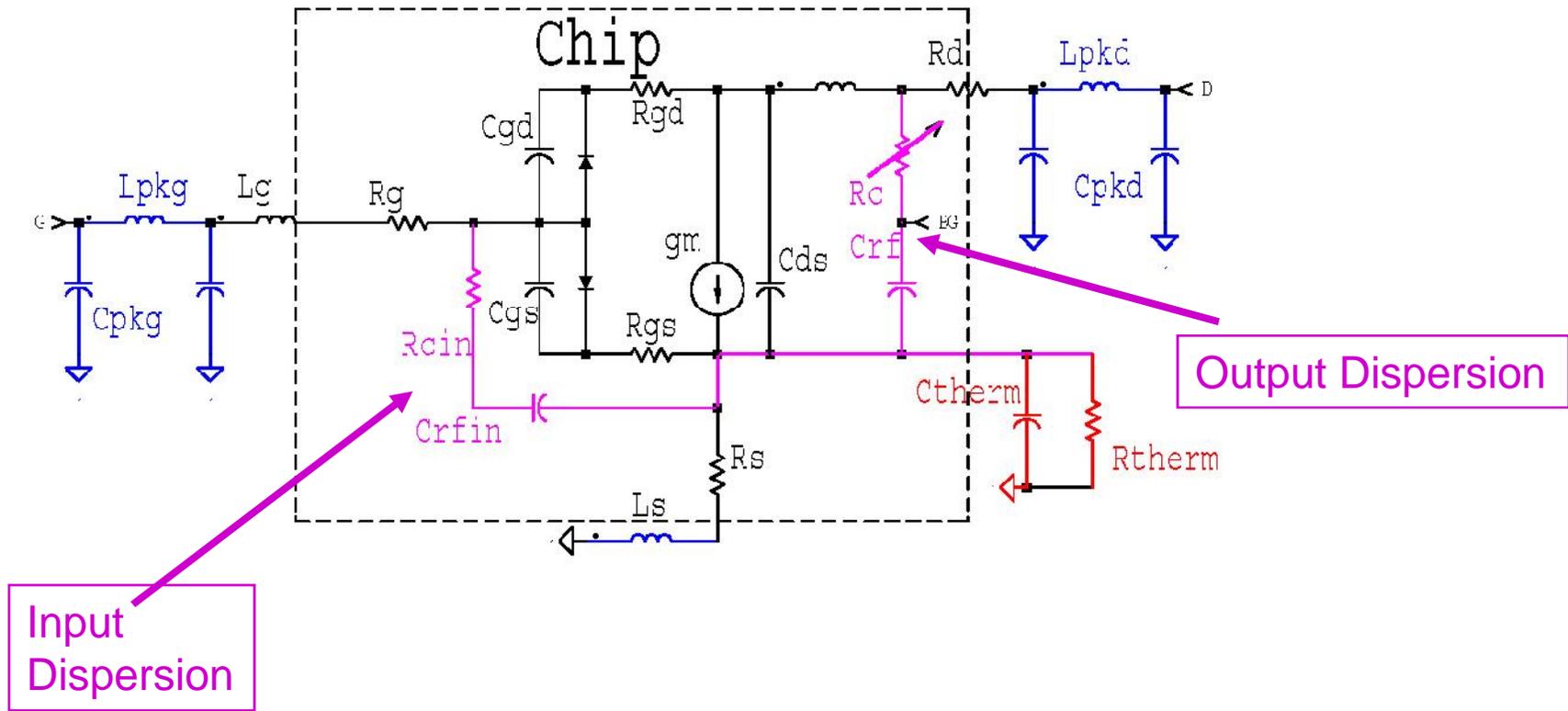
 - DC Output Characteristic i_d - v_{ds}

 - Thermal Modeling

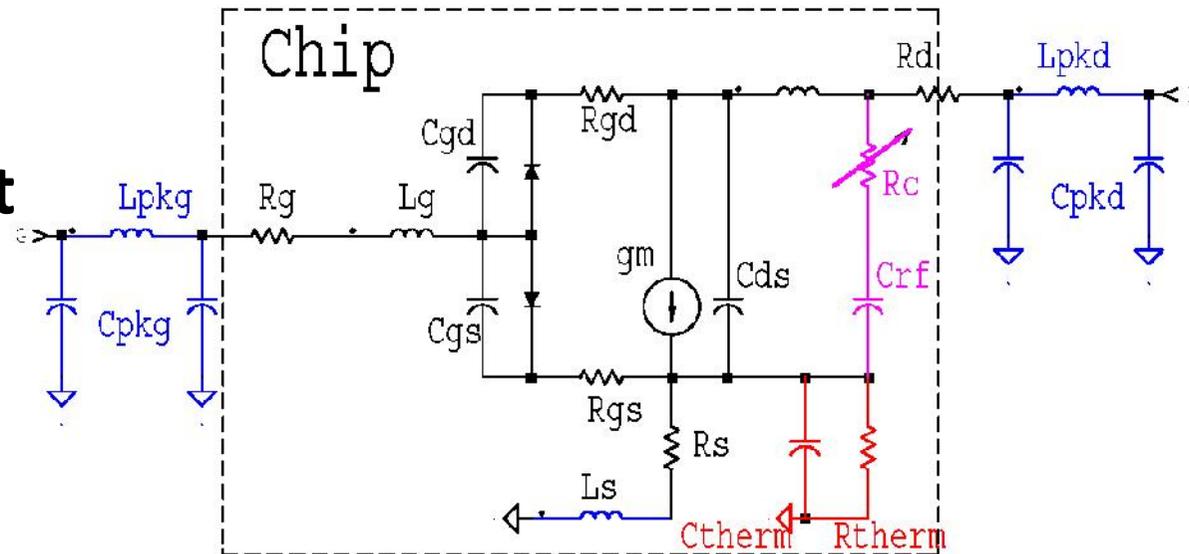
 - S-Parameter Modeling

- **Modeling Results**

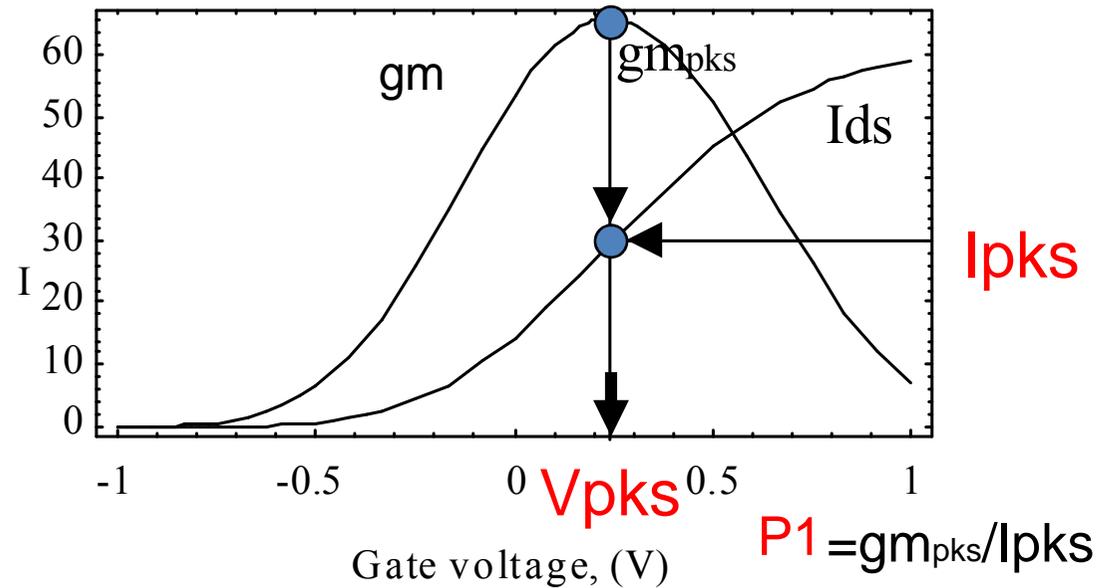
Angelov Model Circuit



FET Equivalent Circuit



The Angelov model features parameter initialization from measurement inspections



Ids equations

$$I_{ds} = I_{pk} (1 + \tanh(\Psi_p)) \tanh(r V_{ds}) (1 + \beta V_{ds} + \beta_{sb} e^{V_{dg} - V_{tr}});$$

$$\mathcal{E}_p = P_{1m} ((V_{gs} - V_{pk0}) + P_2 (V_{gs} - V_{pks})^2 + P_3 (V_{gs} - V_{pkm})^3);$$

$$P_{1m} = g_{mpk} / I_{pk};$$

$$V_{pk}(V_{ds}) = V_{pk0} + \Delta V_{pks} \tanh(r_s V_{ds}) - V_{sb2} (V_{dg} - V_{tr})^2;$$

$$r = r_r + r_s [1 + \tanh(\mathcal{E}_p)]; P_{1m} = P_{1s} (1 + B_1 / \cosh(B_2 V_{ds}));$$

$$I_{ds} = I_{dsp} - I_{dsn}; \quad \text{Symmetric model}$$

$$I_{dsp} = I_{pk} (1 + \tanh(\Psi_p)) (1 + \tanh(r V_{ds})) (1 + \beta V_{ds} + \beta_{sb} e^{V_{dg} - V_{tr}});$$

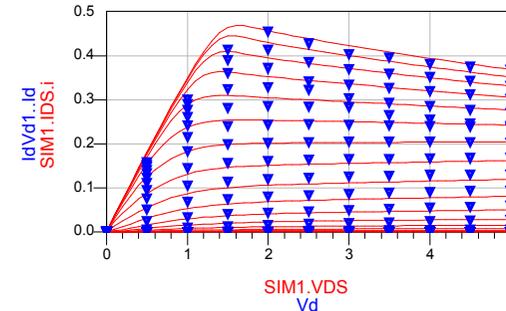
$$I_{dsn} = I_{pk} (1 + \tanh(\Psi_n)) (1 - \tanh(r V_{ds})) (1 - \beta V_{ds});$$

$$\mathcal{E}_p = P_{1m} ((V_{gs} - V_{pk0}) + P_2 (V_{gs} - V_{pks})^2 + P_3 (V_{gs} - V_{pkm})^3);$$

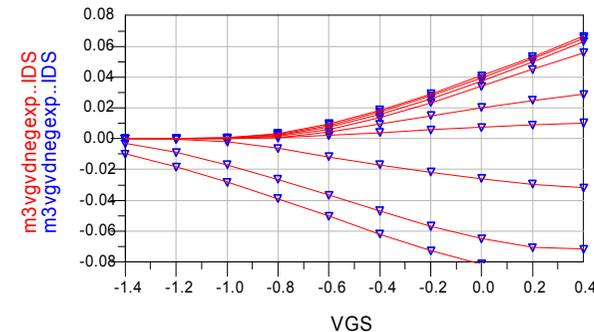
$$\mathcal{E}_n = P_{1m} ((V_{gd} - V_{pk0}) + P_2 (V_{gd} - V_{pks})^2 + P_3 (V_{gd} - V_{pkm})^3);$$

$$r = r_r + r_s [1 + \tanh(\mathcal{E}_n)];$$

FET Current source:
The ideal case is if we can split:
 $I_{ds} = f_1(V_{gs}) * f_2(V_{ds})$



High Power FET Measured&Model



Symmetrical model
Meas.&Model

Gate Charge

• Capacitance implementation

$$1 \rightarrow \frac{\partial V_{gs}}{\partial t}; \frac{\partial V_{gd}}{\partial t}; 2 \rightarrow I_{gs} = \frac{\partial V_{gs}}{\partial t} C_{gs}; I_{gd} = \frac{\partial V_{gd}}{\partial t} C_{gd};$$

$$C_{gs} = C_{gsp} + C_{gs0} \cdot (1 + \tanh[\xi_1]) \cdot (1 + \tanh[\xi_2])$$

$$\xi_1 = P_{10} + P_{11} \cdot V_{gs} + P_{111} \cdot V_{ds}; \xi_2 = P_{20} + P_{21} \cdot V_{ds};$$

$$C_{gd} = C_{gdp} + C_{gd0} \cdot (1 + \tanh[\xi_3]) \cdot (1 + \tanh[\xi_4] + 2P_{111})$$

$$\xi_3 = P_{30} - P_{31} \cdot V_{ds}; \xi_4 = P_{40} + P_{41} \cdot V_{gd} - P_{111} \cdot V_{ds};$$

P_{111} -high voltage effects for C_{gs} & cross-coupling for C_{gd}

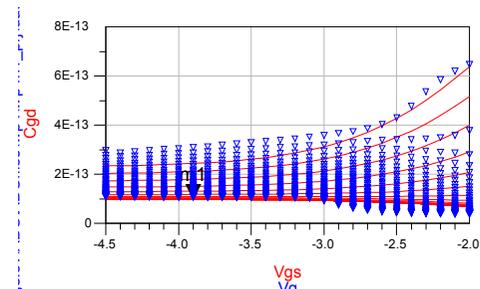
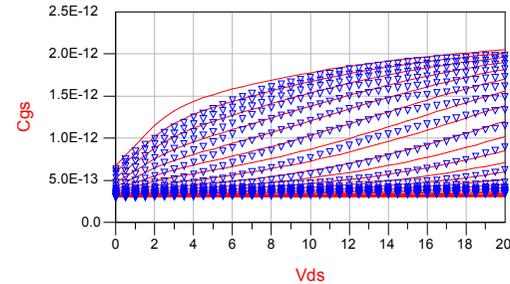
$$Q_g = Q_{gs} + Q_{gd};$$

• Charge implementation

$$Q_{gs} = \int C_{gs}(V_{gs}, V_{ds}) dV_{gs} = C_{gsp} \cdot V_{gs} + C_{gs0} \cdot (V_{gs} + Lc1) Th2;$$

$$Q_{gd} = \int C_{gd}(V_{gs}, V_{gd}) dV_{gd} = C_{gdp} \cdot V_{gd} + C_{gd0} \cdot (V_{gd} + Lc4) Th3;$$

$$Lc1 = \frac{\log[\cosh[\xi_1]]}{P_{11}}, Th2 = \tanh[\xi_2]; Lc4 = \frac{\log[\cosh[\xi_4]]}{P_{41}}, Th3 = \tanh[\xi_3]$$



Outline

- Introduction to the Angelov Model

- **Step-by-Step Modeling Sequence**

 - Resistances R_G , R_D , R_S

 - DC Input Characteristic i_g - v_{gs}

 - DC Transfer Characteristic i_d - v_{gs}

 - DC Output Characteristic i_d - v_{ds}

 - Thermal Modeling

 - S-Parameter Modeling

- **Modeling Results**

Angelov Modeling Flow:

-1- RS, RD

-2- $ig(vg)$

-3- $id(vg)$

-4- $id(vd)$

-5- S-parameters: RG, Inductors

capacitors from $vd-vd$ and $vd-vg$ biasing

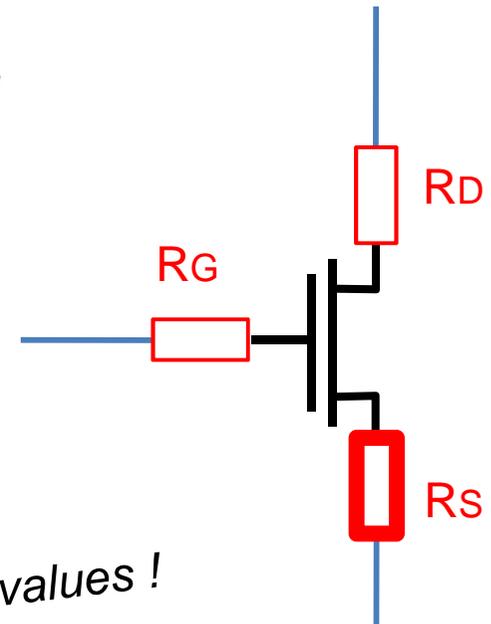
-6- Nonlin-RF: fine-tuning & verification

Resistances R_G , R_D , R_S



The accurate extraction of the external resistors is extremely important for a successful device modeling, because they strongly affect the remaining inner model performance.

Of particular importance is R_S :
a wrong R_S value affects basically all DC parameter values !



As a best-practice, the external resistors values are extracted applying different extraction methods.

FROM DC:

- **RD** from id-vd linear range
- **RS** from id-vd: distribution of id curves for vd in saturation or from DC Flyback measurement

FROM S-PARAMETERS:

- **RS, RG, RD** from ColdFET (Dambrine*)

Once these resistors are modeled, and during the remaining modeling steps:

- RS should be changed only very little
- RG will be tuned to fit S11
- RD will be tuned to fit id-vd in the linear range

* G.Dambrine et.al., 'A New Method for Determining the FET Small-Signal Equivalent Circuit', IEEE Trans.Microwave Theory and Techniques, vol.36, nr.7, July 1988

➤ Step-by-Step Modeling Sequence

Resistances R_G , R_D , R_S

DC Input Characteristic ig - vgs

DC Transfer Characteristic id - vgs

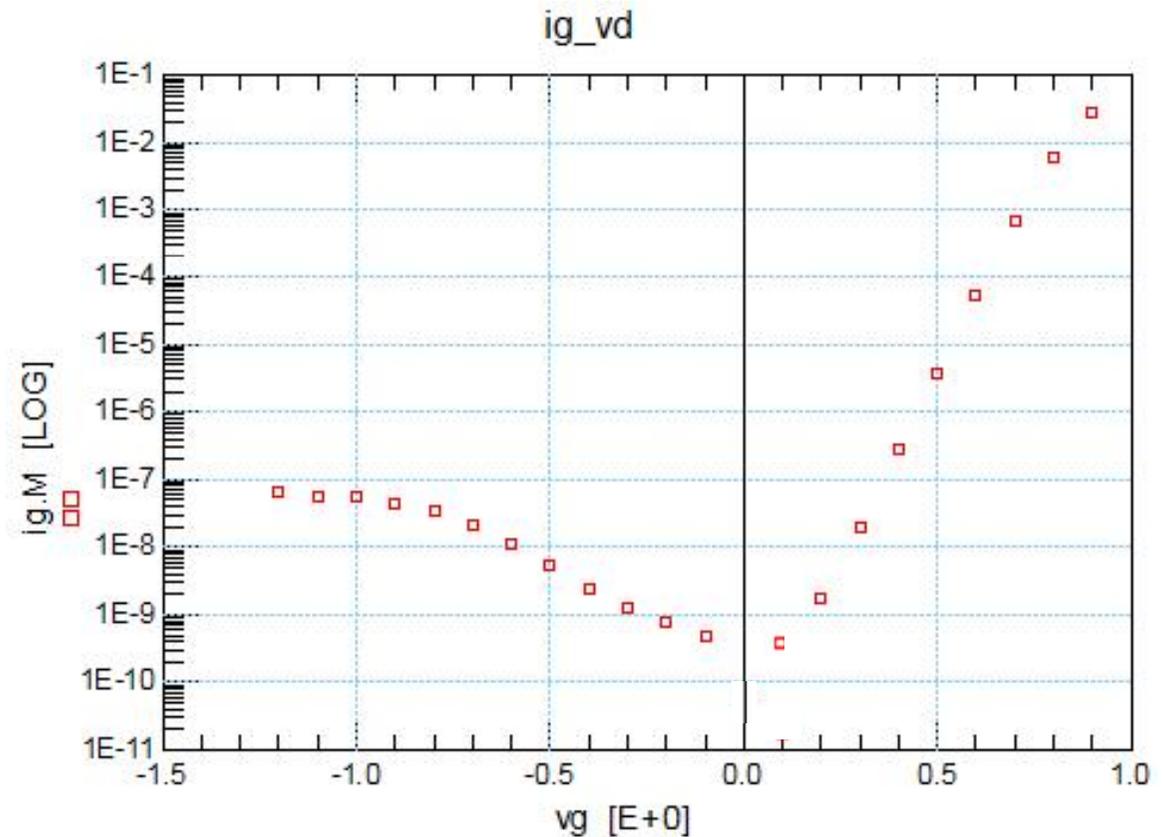
DC Output Characteristic id - vds

Thermal Modeling

S-Parameter Modeling

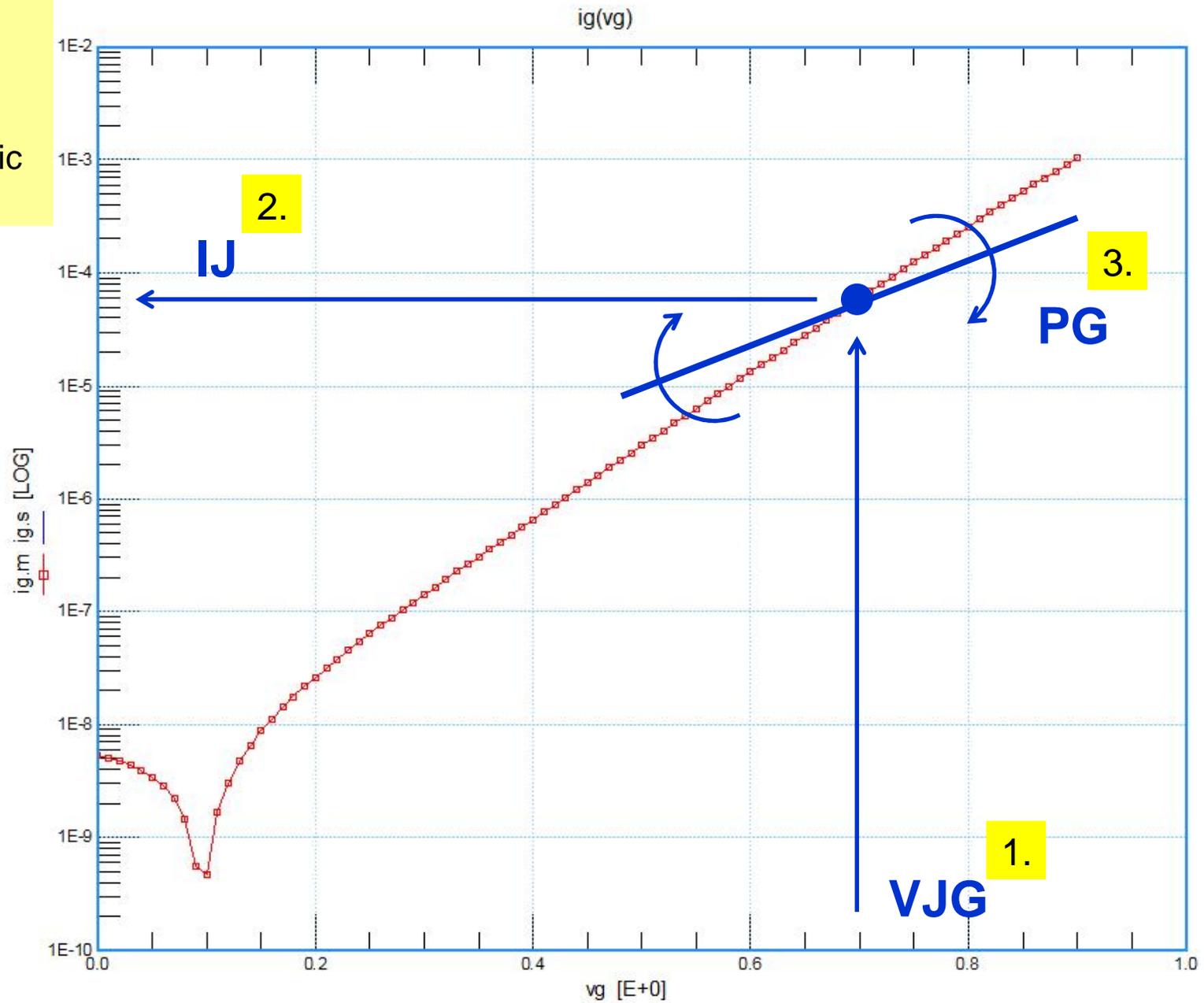
DC Input Characteristic

ig vs. v_g



ig vs. vg

Modeling the diode characteristic for $v_g > 0$



➤ **Step-by-Step Modeling Sequence**

Resistances R_G , R_D , R_S

DC Input Characteristic $ig-vgs$

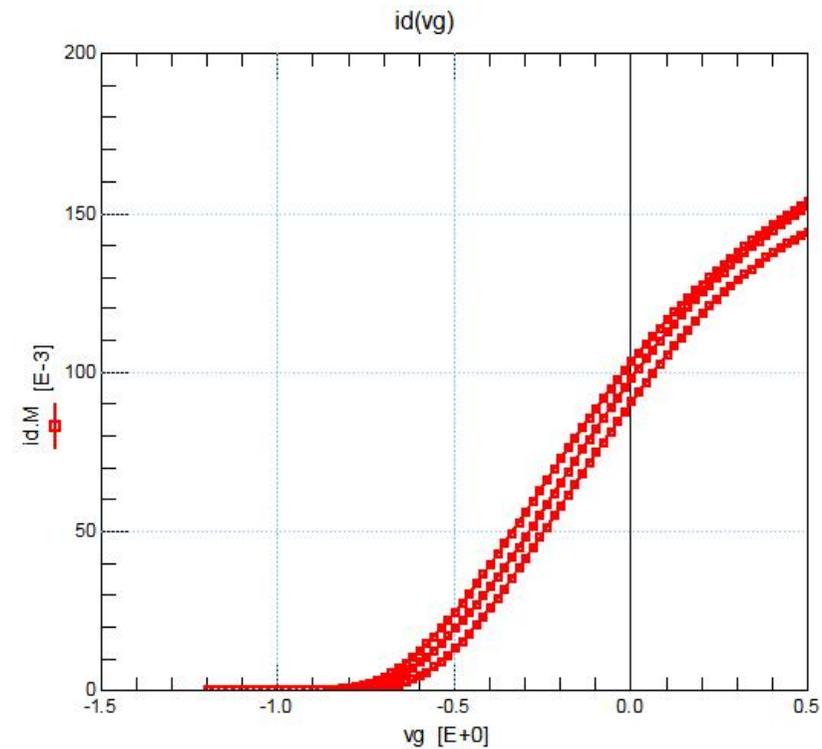
DC Transfer Characteristic $id-vgs$

DC Output Characteristic $id-vds$

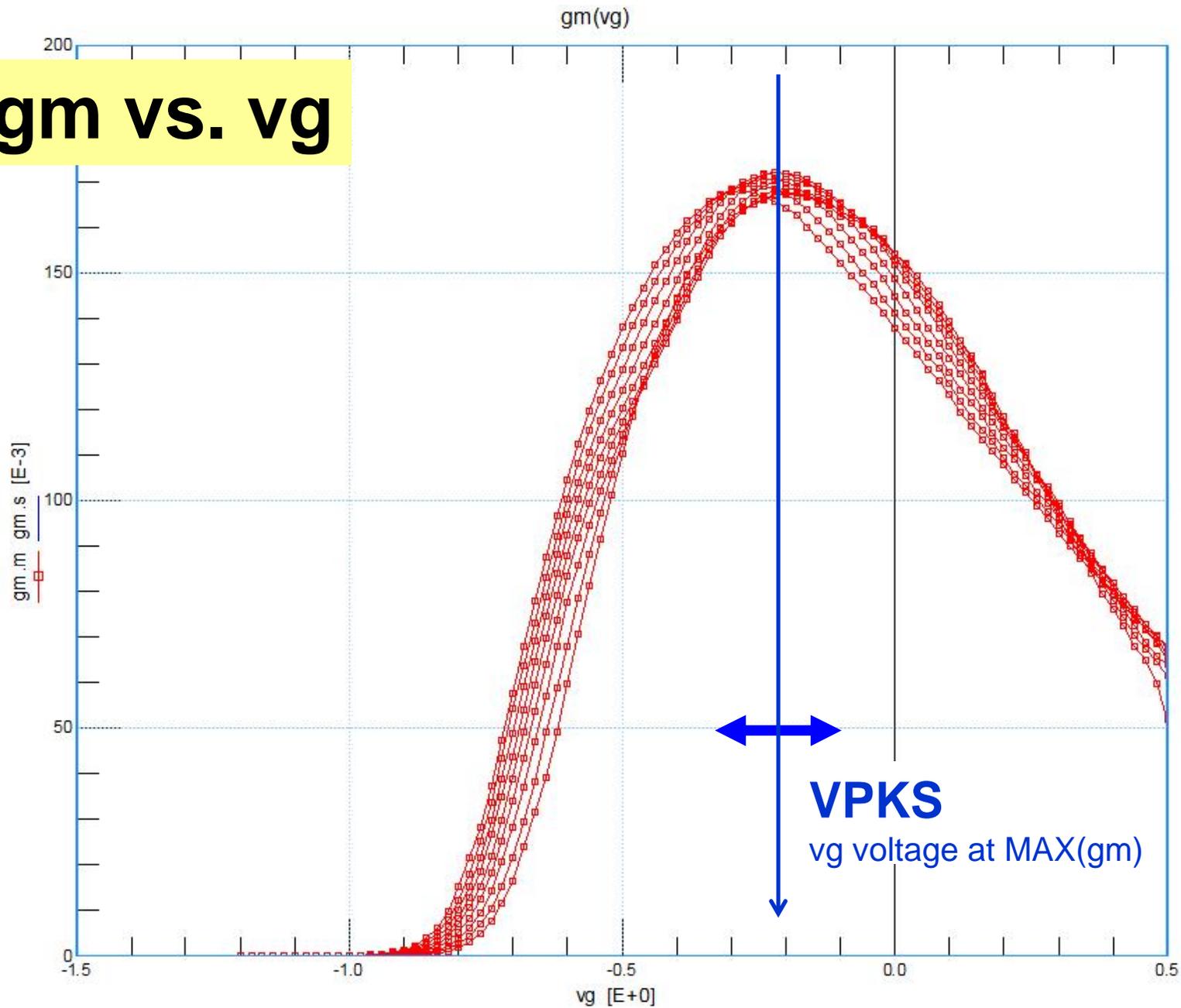
Thermal Modeling

S-Parameter Modeling

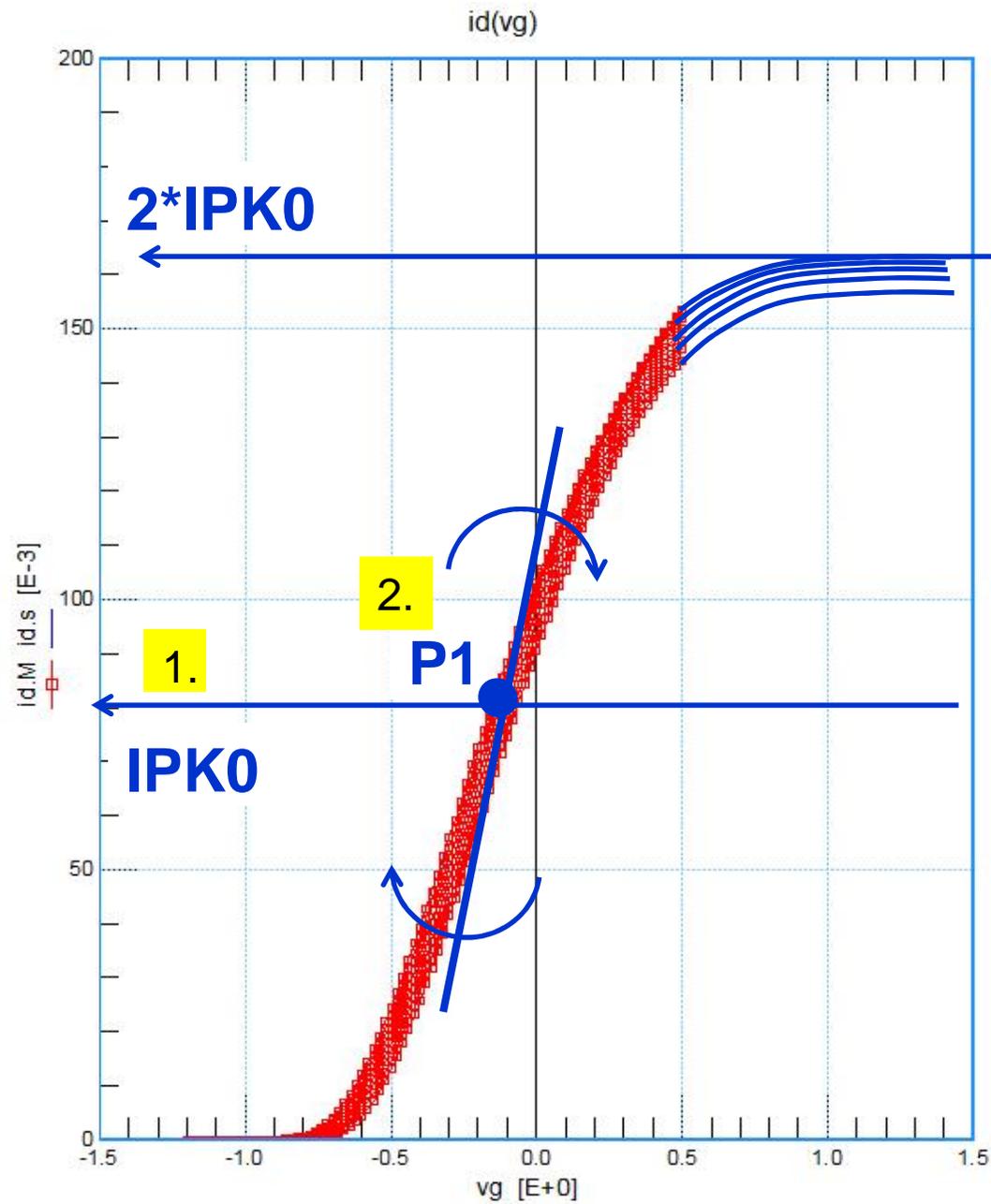
DC Transfer Characteristic id vs. vg



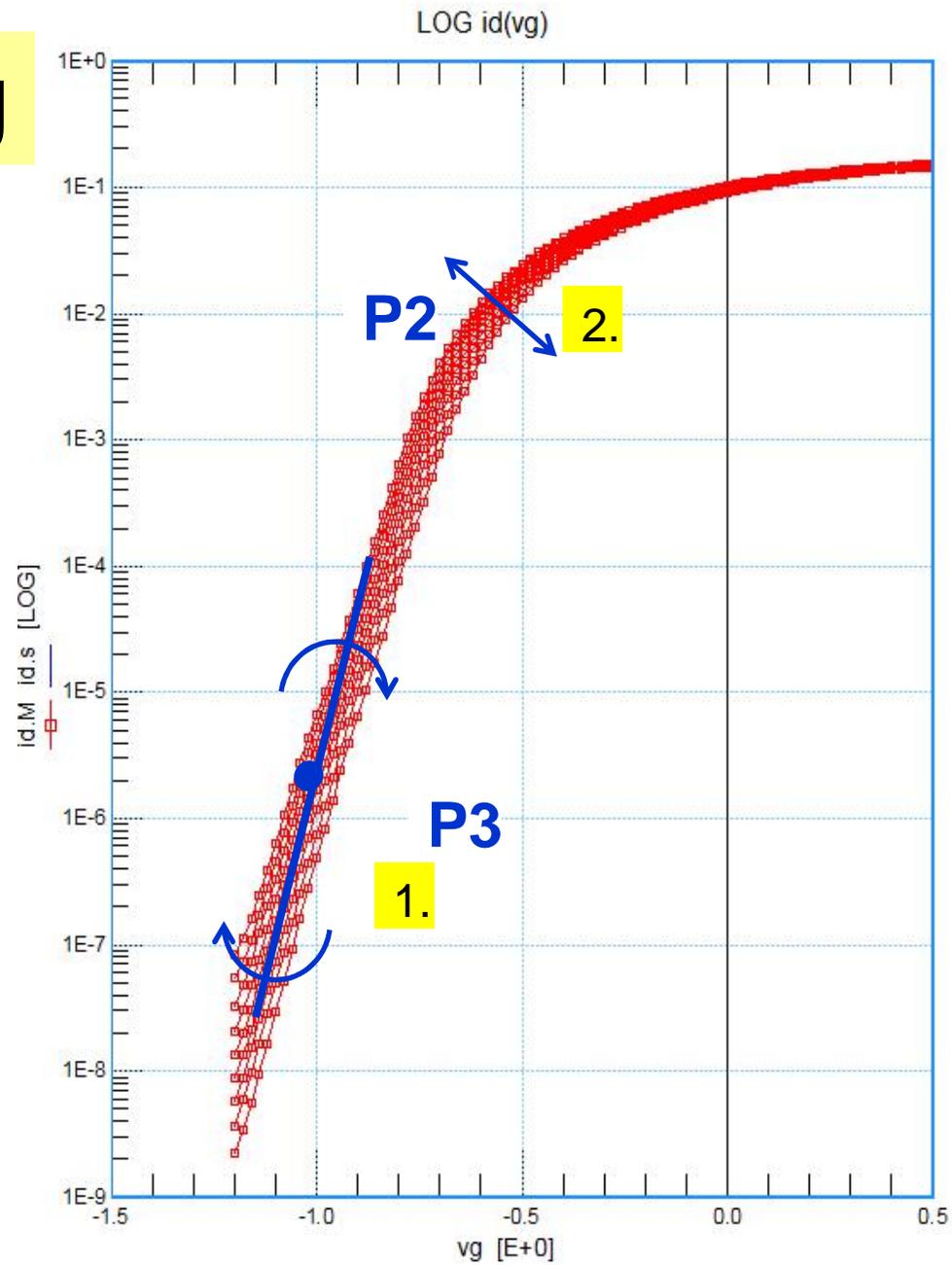
gm vs. vg



id vs. vg

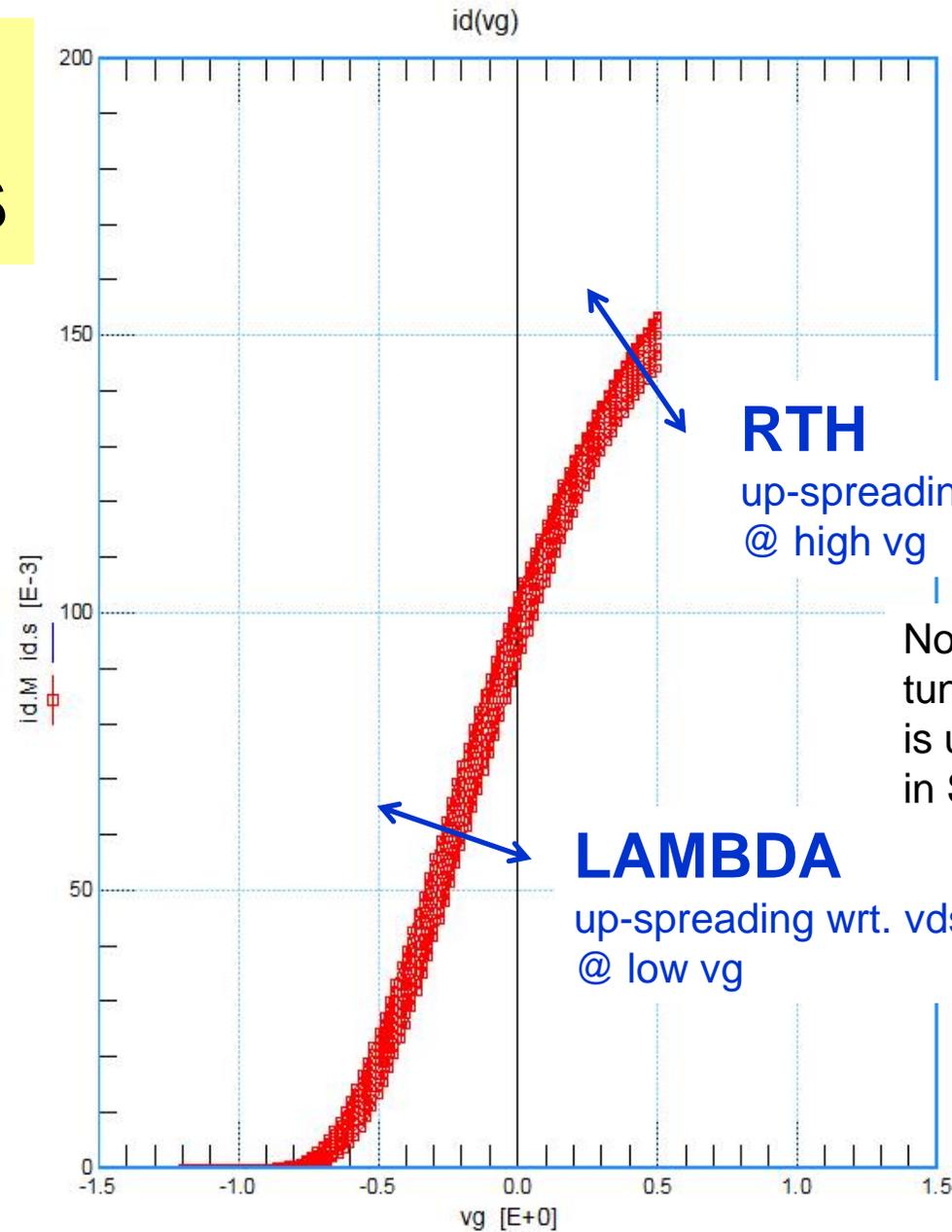


LOG(id) vs.vg



id vs. vgs

Effect of vds



RTH

up-spreading wrt. vds,
@ high v_g

Note:

tuning RTH and LAMBDA
is usually more obvious
in Setup id-vd

LAMBDA

up-spreading wrt. vds,
@ low v_g

➤ **Step-by-Step Modeling Sequence**

Resistances R_G , R_D , R_S

DC Input Characteristic i_g - v_{gs}

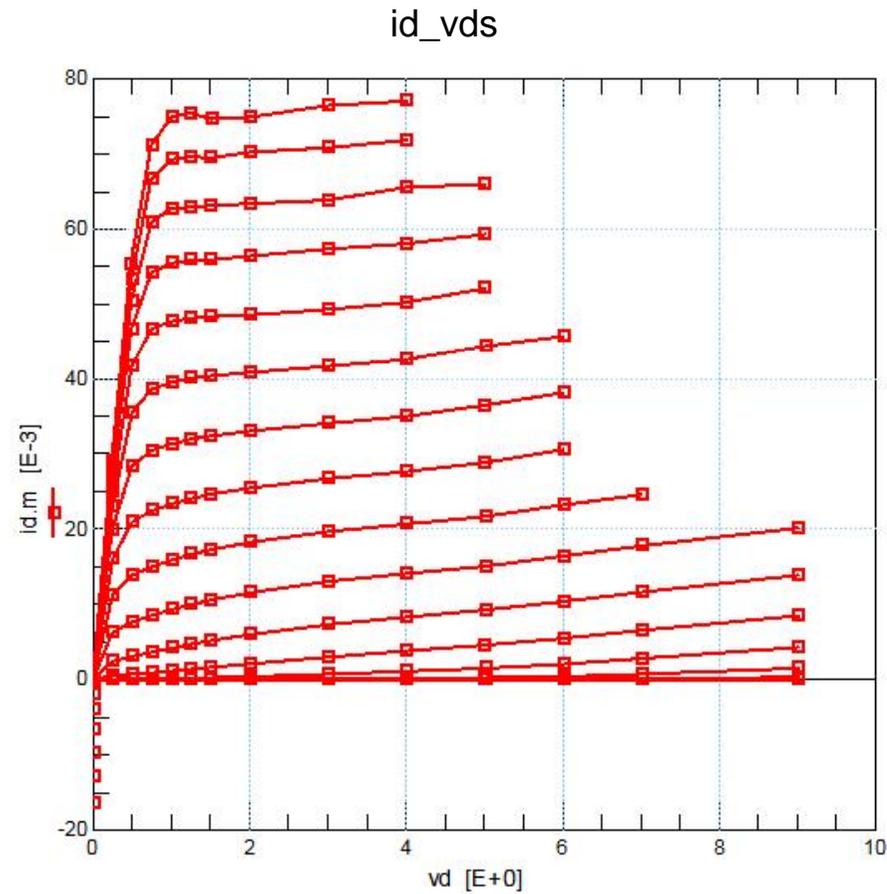
DC Transfer Characteristic i_d - v_{gs}

DC Output Characteristic i_d - v_{ds}

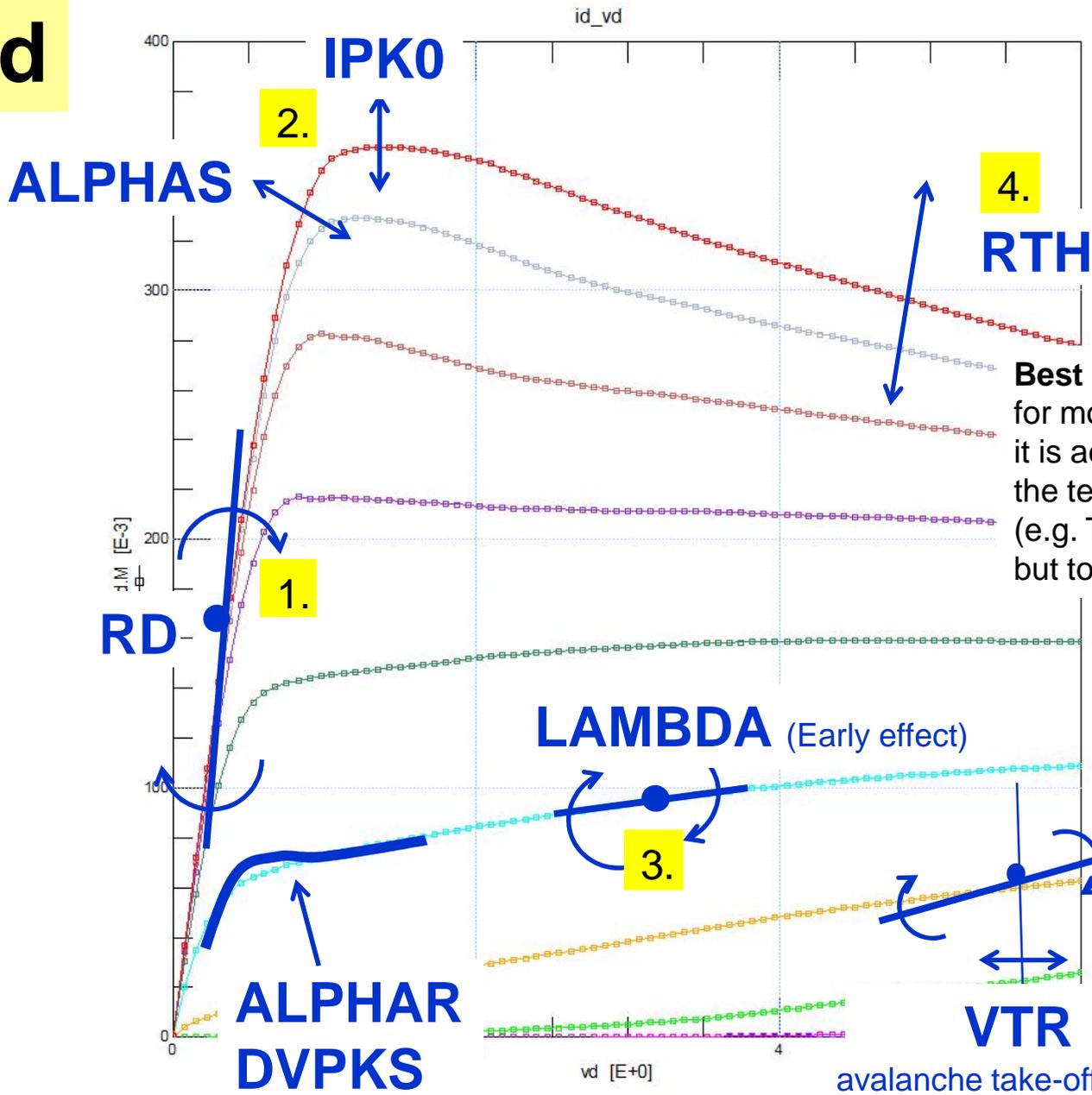
Thermal Modeling

S-Parameter Modeling

DC Output Characteristic i_d vs. v_d

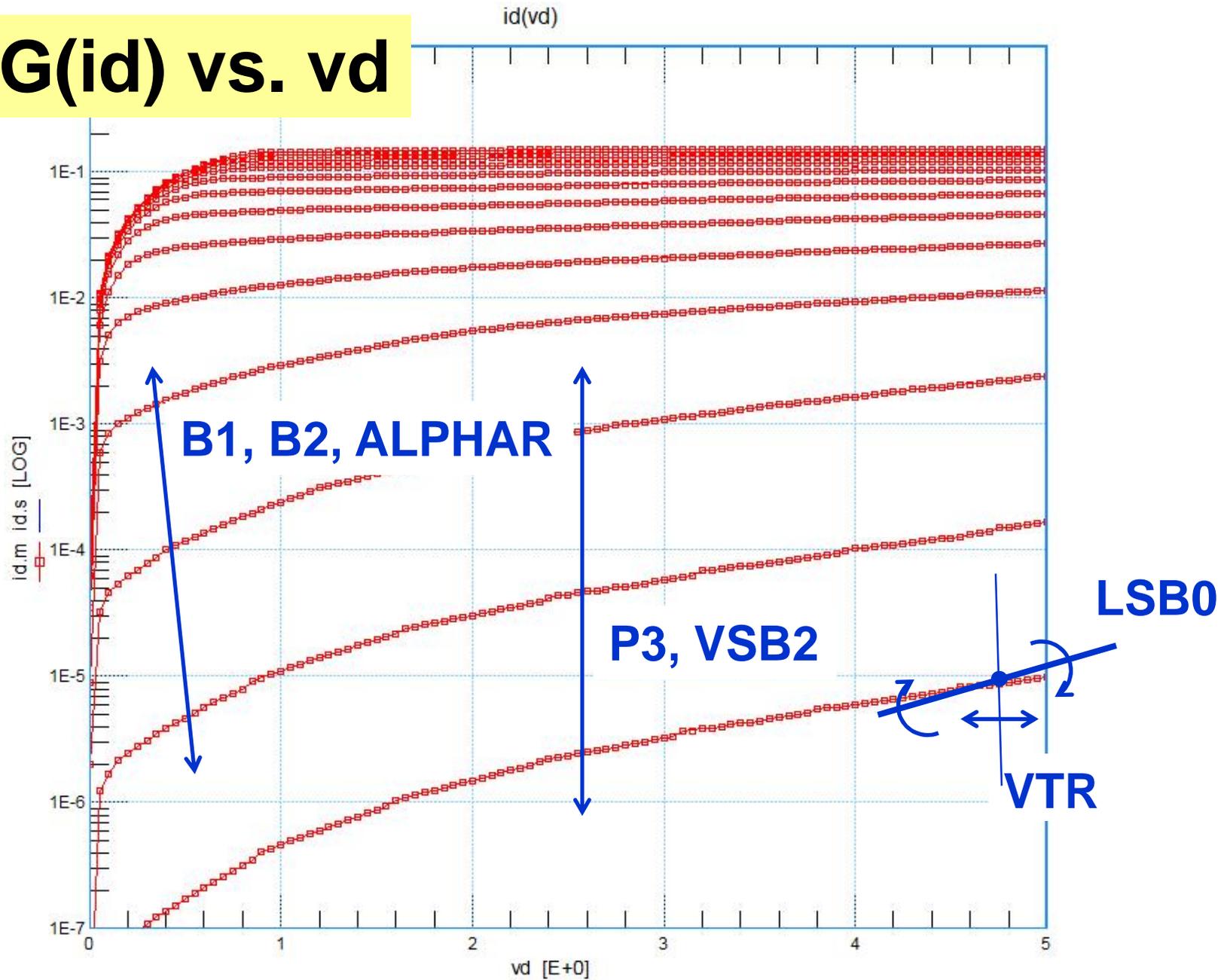


id vs. vd



Best Practice Notice:
for model stability,
it is advised to not tune
the temp. coeff. parameters
(e.g. TCIPK0, TCP1, etc),
but to keep their default values.

LOG(id) vs. vd



➤ **Step-by-Step Modeling Sequence**

Resistances R_G , R_D , R_S

DC Input Characteristic i_g - v_{gs}

DC Transfer Characteristic i_d - v_{gs}

DC Output Characteristic i_d - v_{ds}

Thermal Modeling

S-Parameter Modeling

A Note on Thermal Modeling

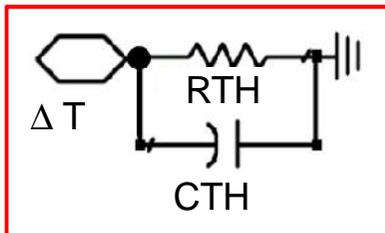
Device Temperature Rise

$$T = R_{TH} * \text{Dissipated_Power}$$

Device Temperature

$$T_{Dev} = TEMP + T$$

thermo-electrical circuit
for the self-heating modeling



CTH models the thermal storage

Usually: $R_{TH} * C_{TH} = 1\text{ms}$

If you don't know CTH, set $C_{TH} = 1\text{E-}3 / R_{TH}$

Never set $C_{TH}=0$!!!



Otherwise, your model is thermally faster than electrically !

➤ **Step-by-Step Modeling Sequence**

Resistances RG, RD, RS

DC Input Characteristic ig-vgs

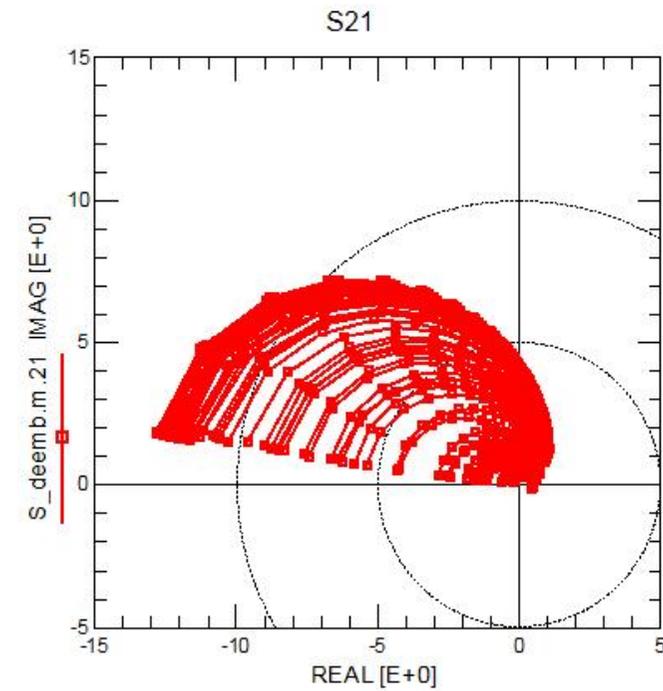
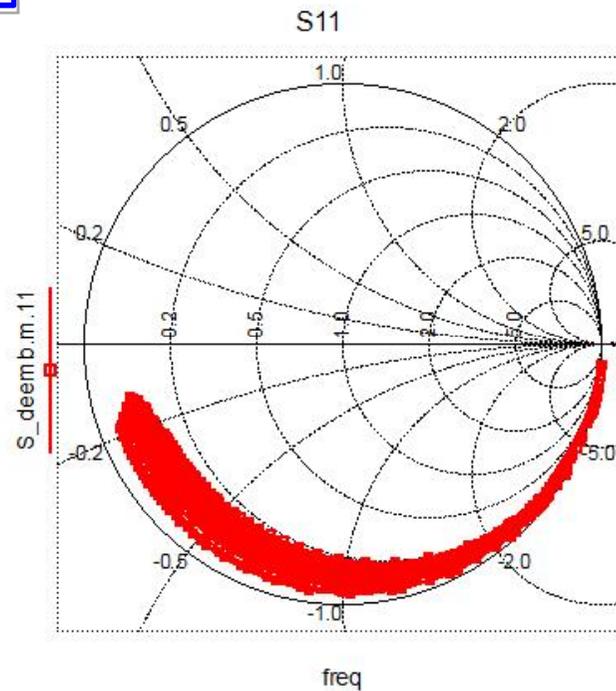
DC Transfer Characteristic id-vgs

DC Output Characteristic id-vds

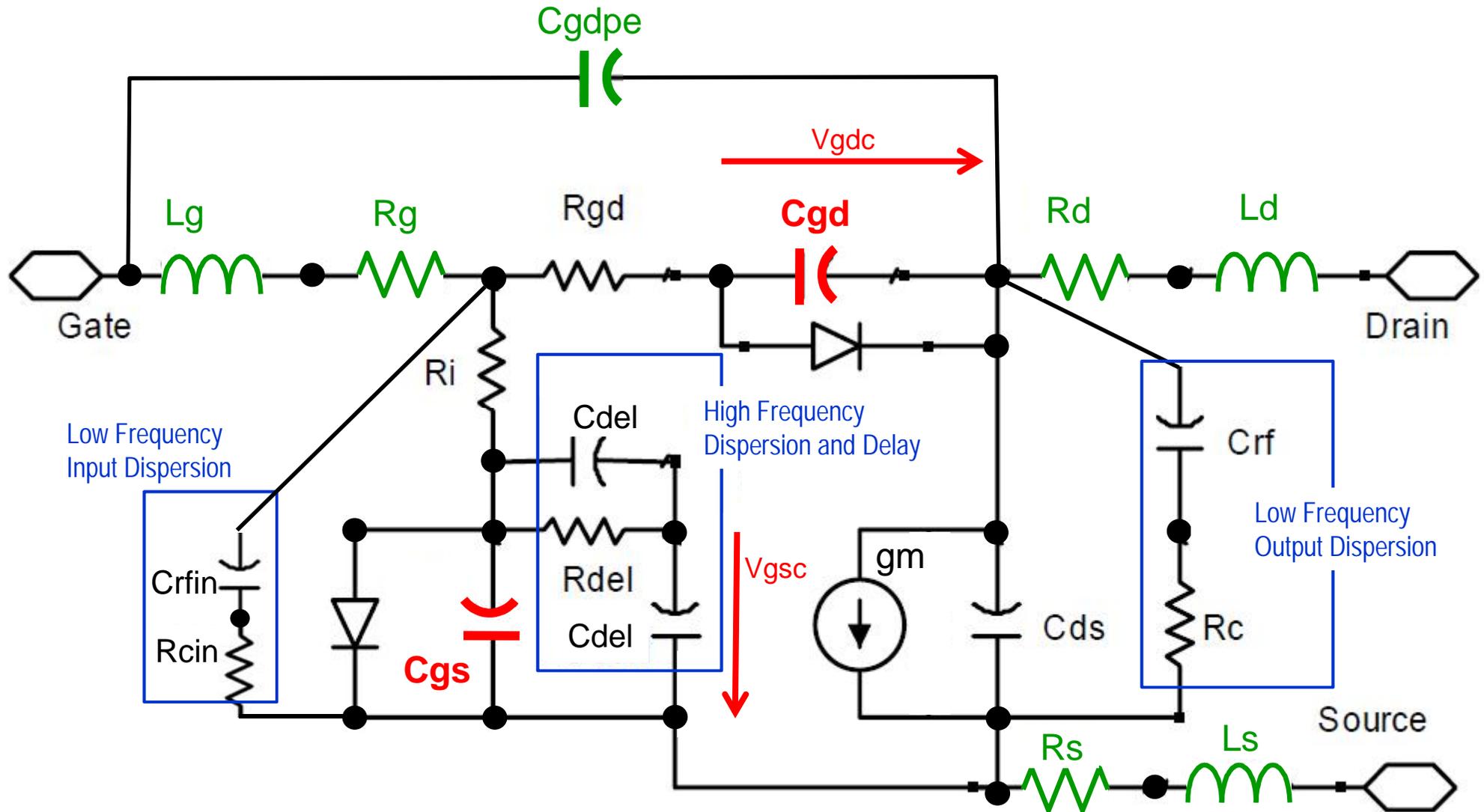
Thermal Modeling

S-Parameter Modeling

S-Parameter Modeling

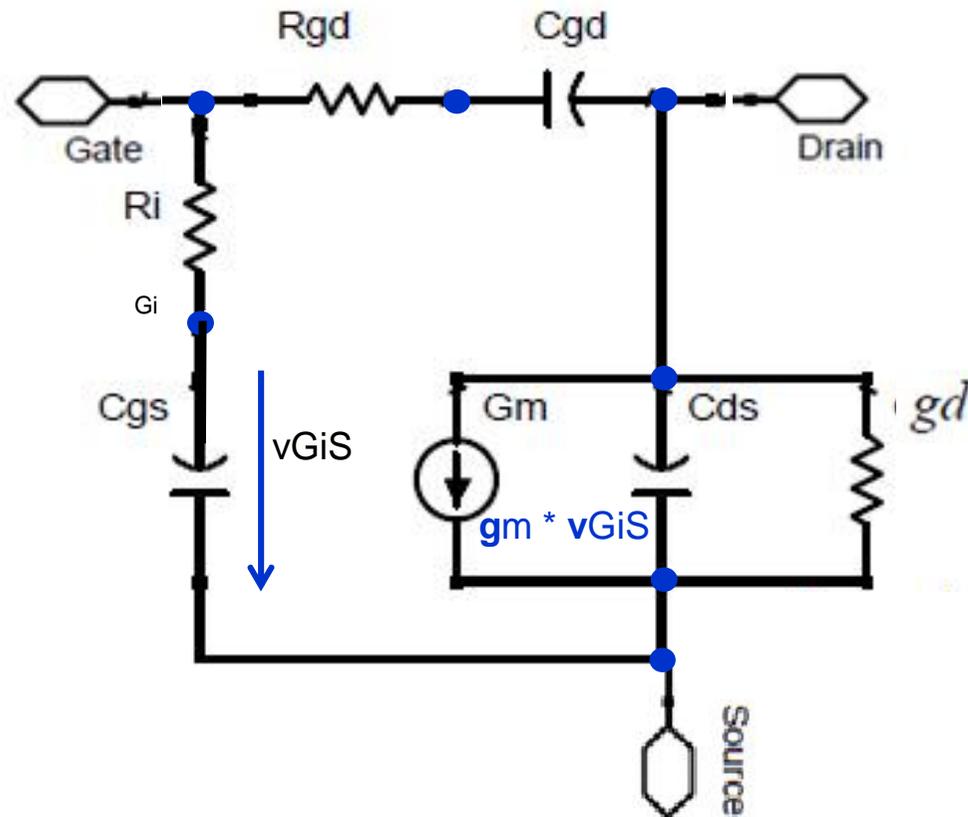


Full AC Schematic



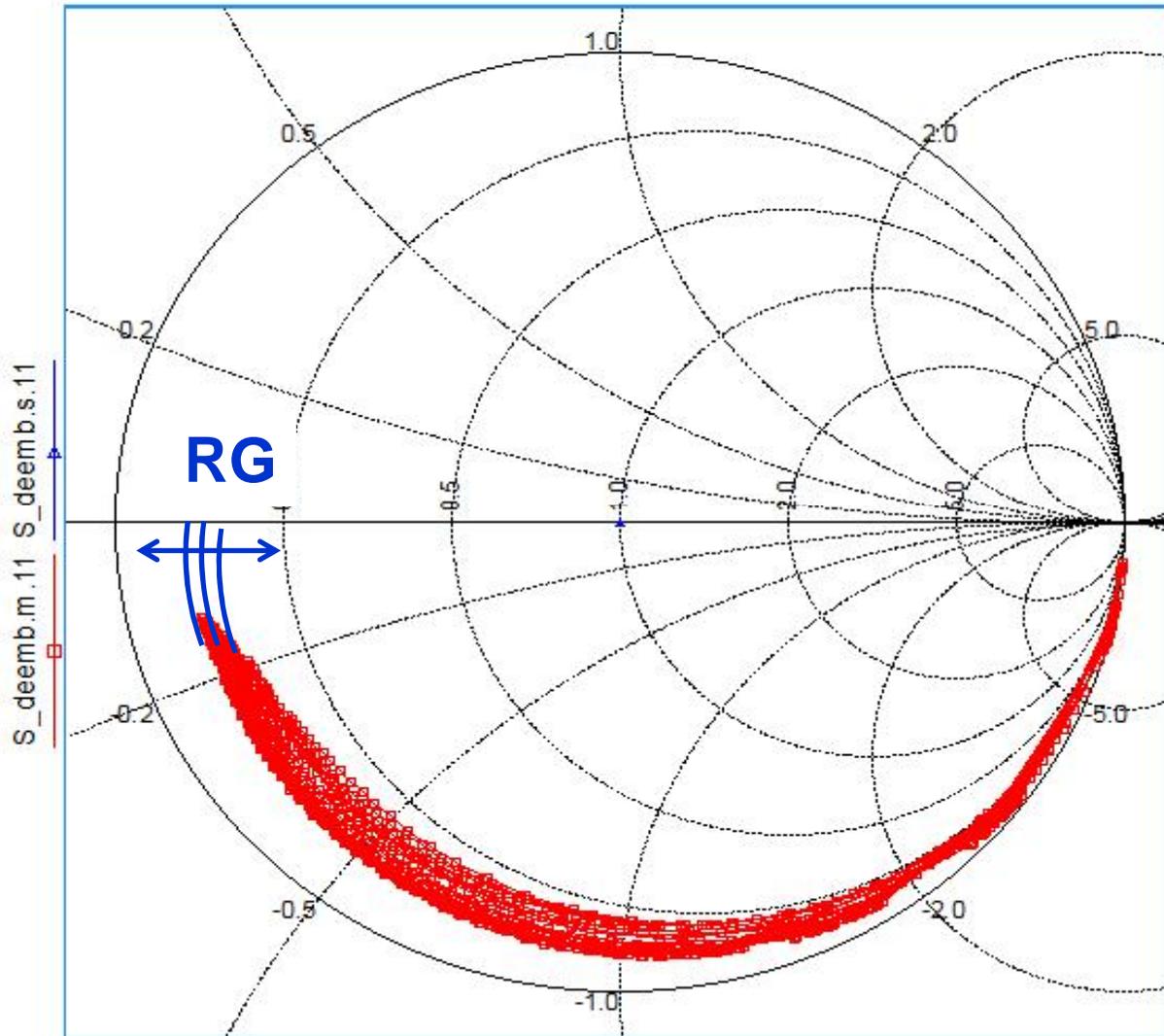
Note: V_{gsc} and V_{gdc} are the internal node control voltages for the bias-dependent capacitances C_{gs} and C_{gd}

Simplified Inner PI AC Schematic

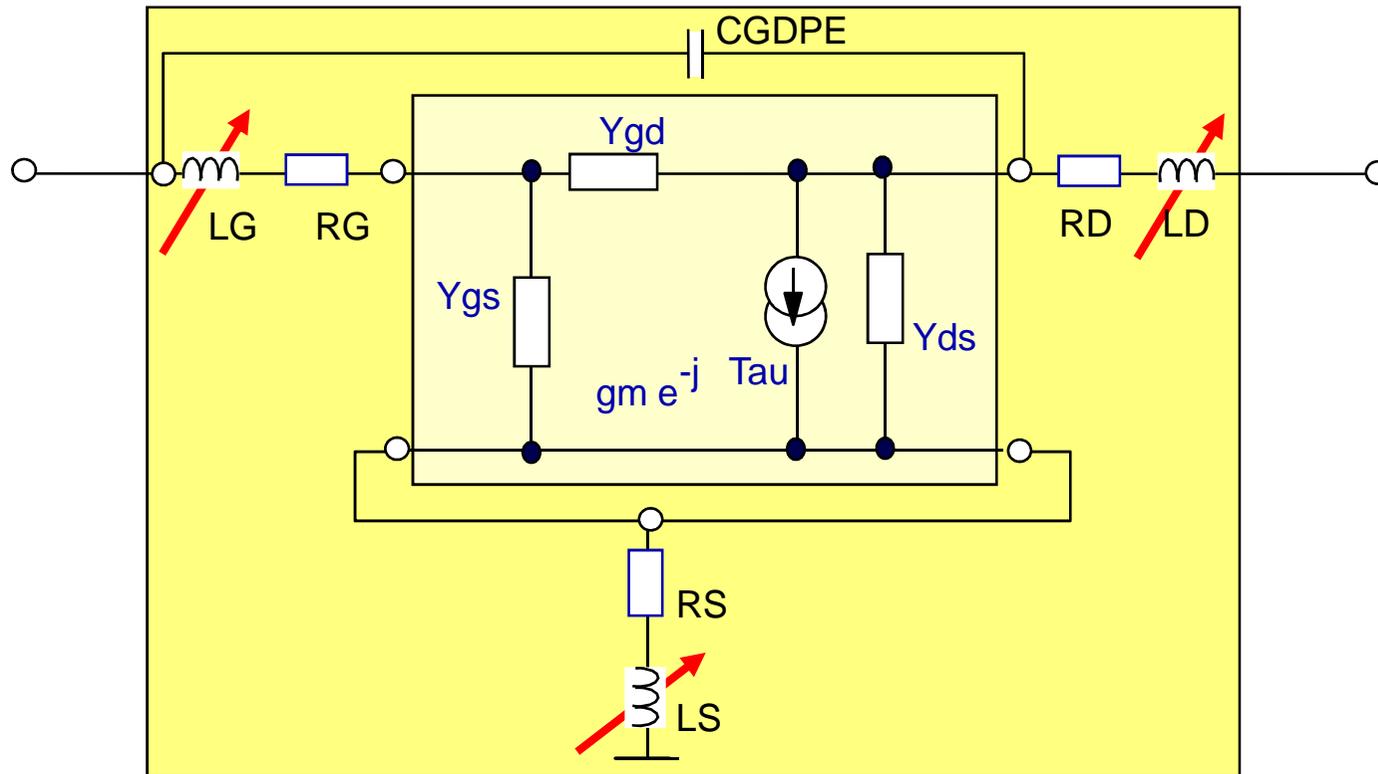


RG

S11

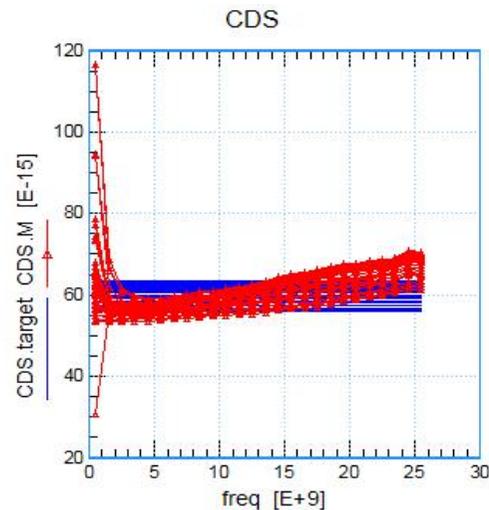
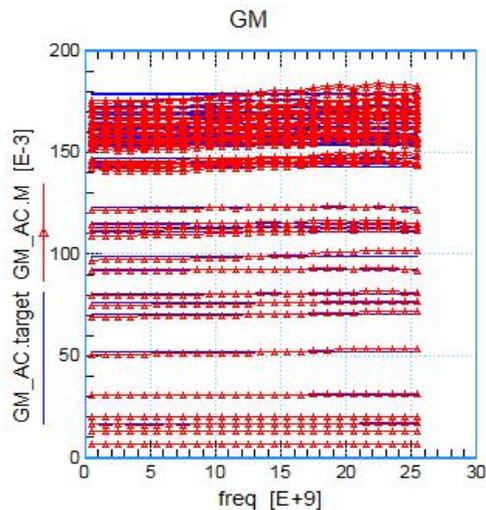
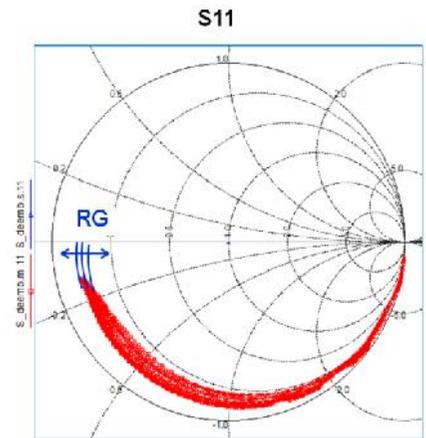
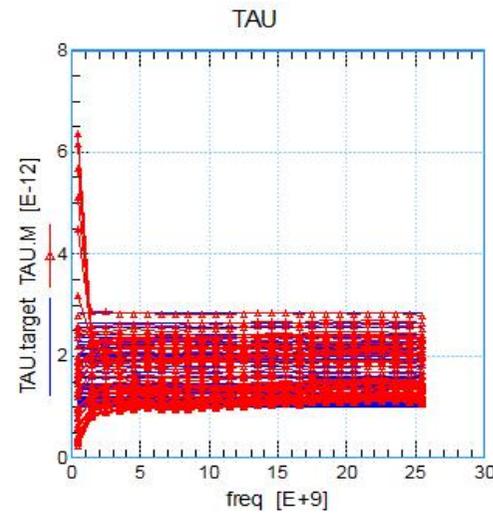
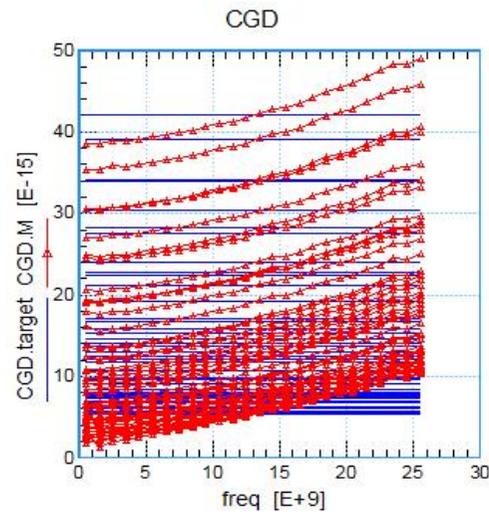
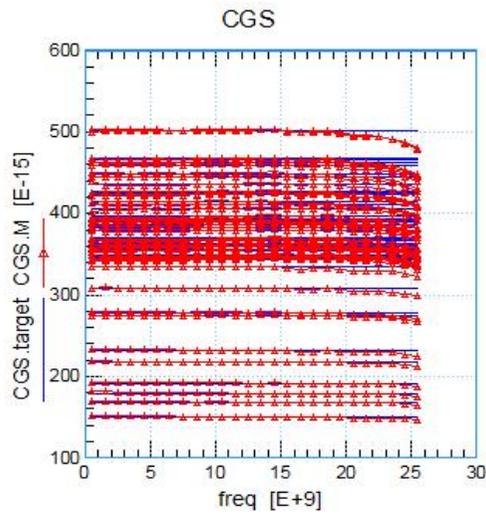


Adjust the extrinsic inductors LG, LD and LS to make intrinsic parameters as freq. independent as possible



For details, see next slide

External Inductors



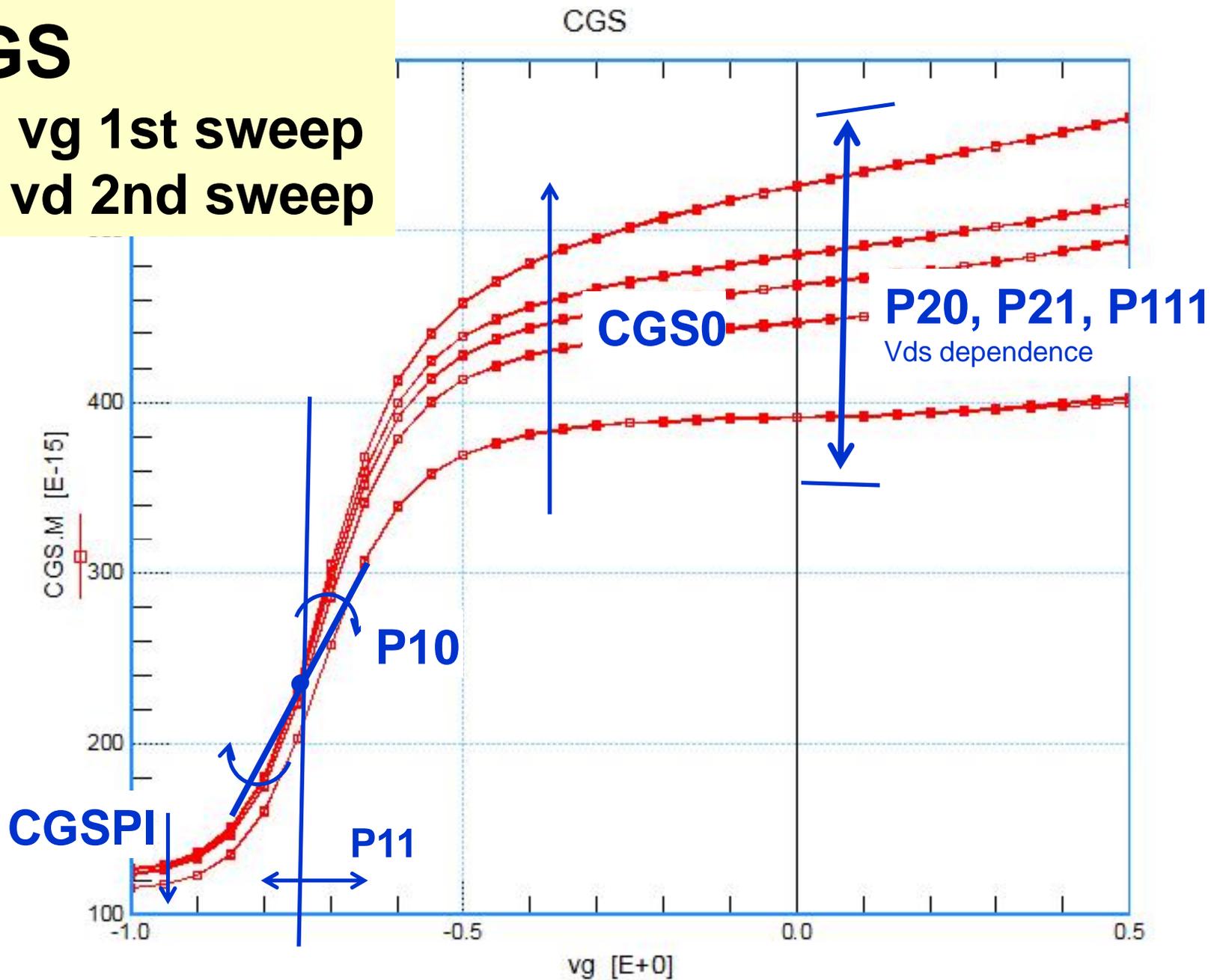
**adjust extrinsic
LG, LD, LS**

**(and also RG, but keep an eye on simulated S11!)
to make the intrinsic parameters
as freq. independent as possible**

Note: RD and RS have been fitted in DC id-vd

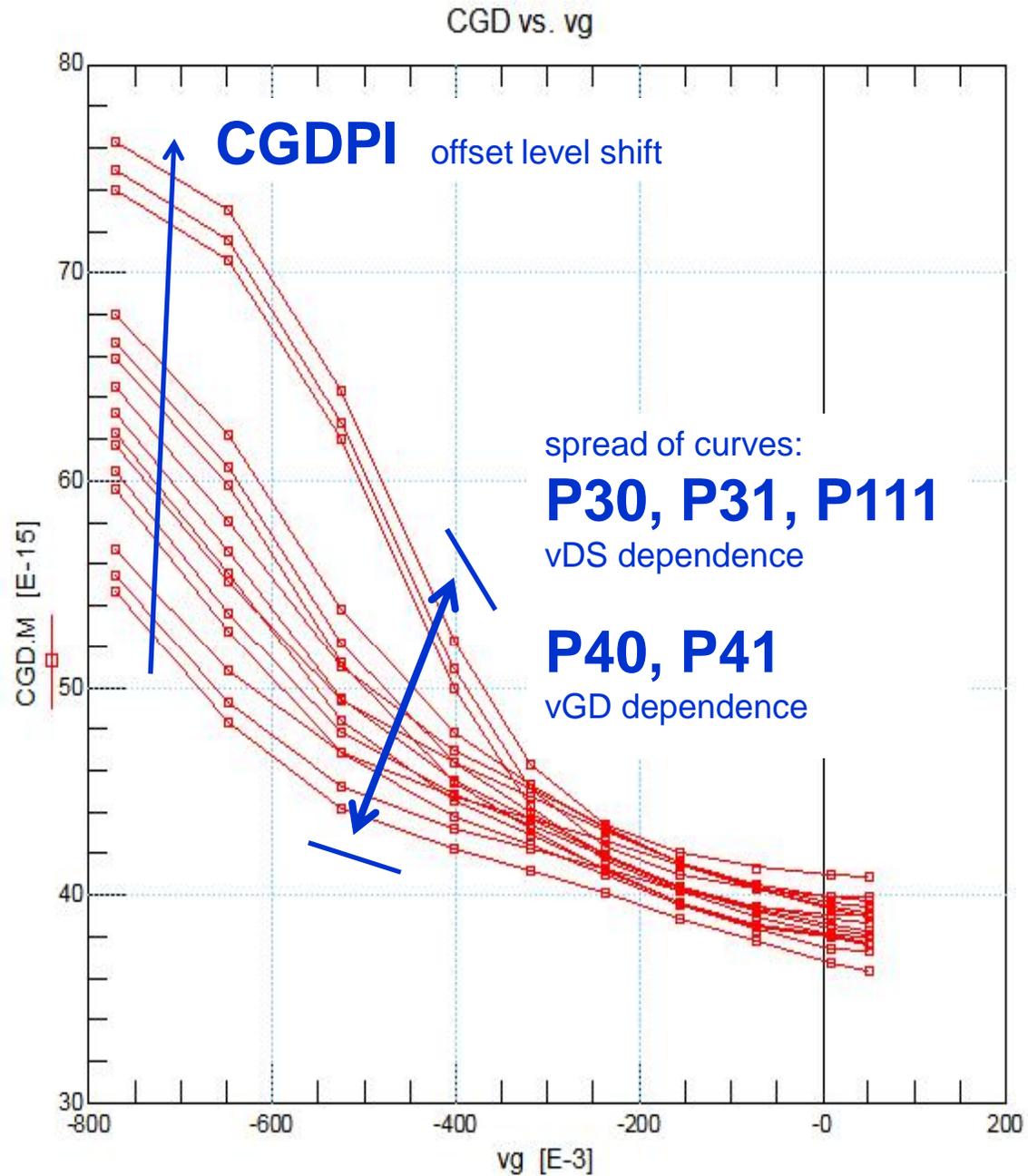
CGS

@ vg 1st sweep
vd 2nd sweep



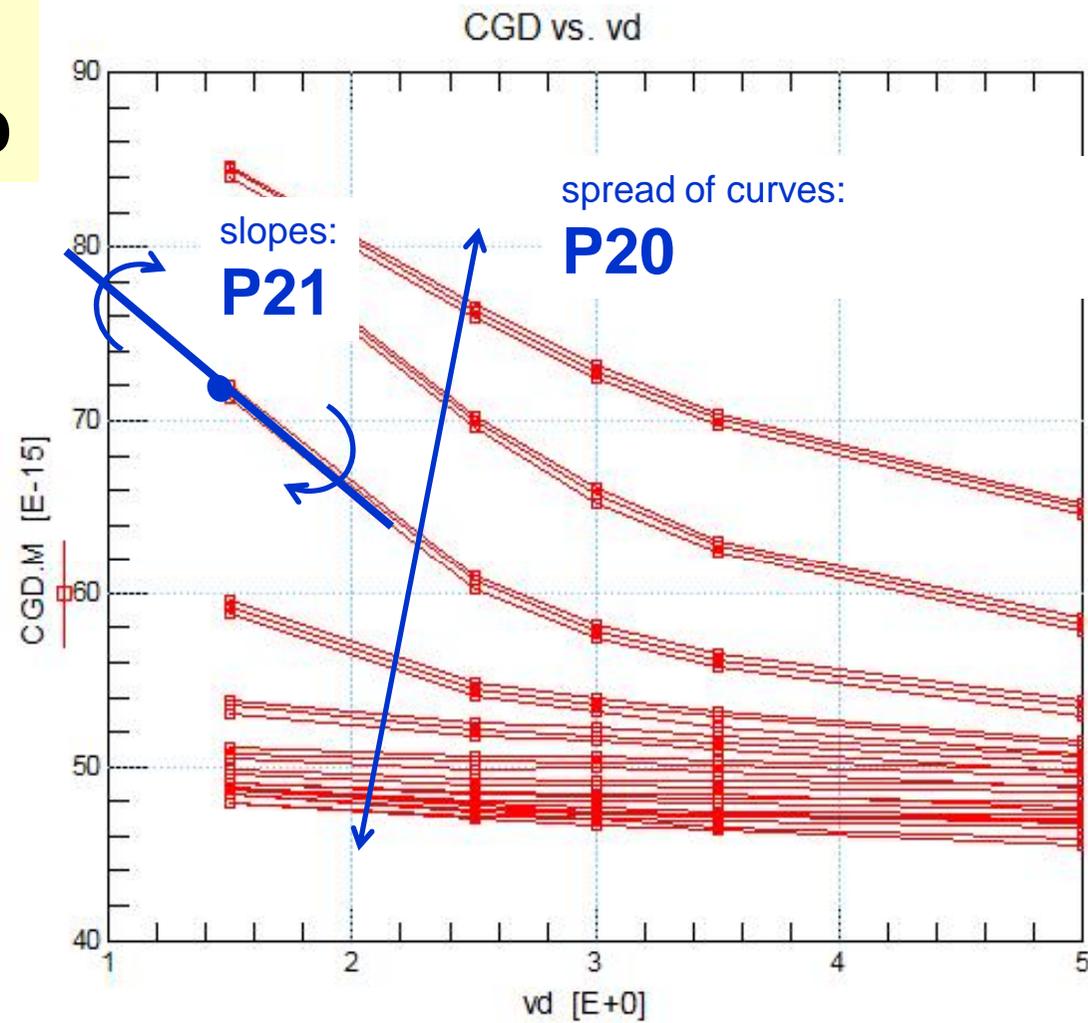
CGD

@ v_g 1st sweep
vd 2nd sweep



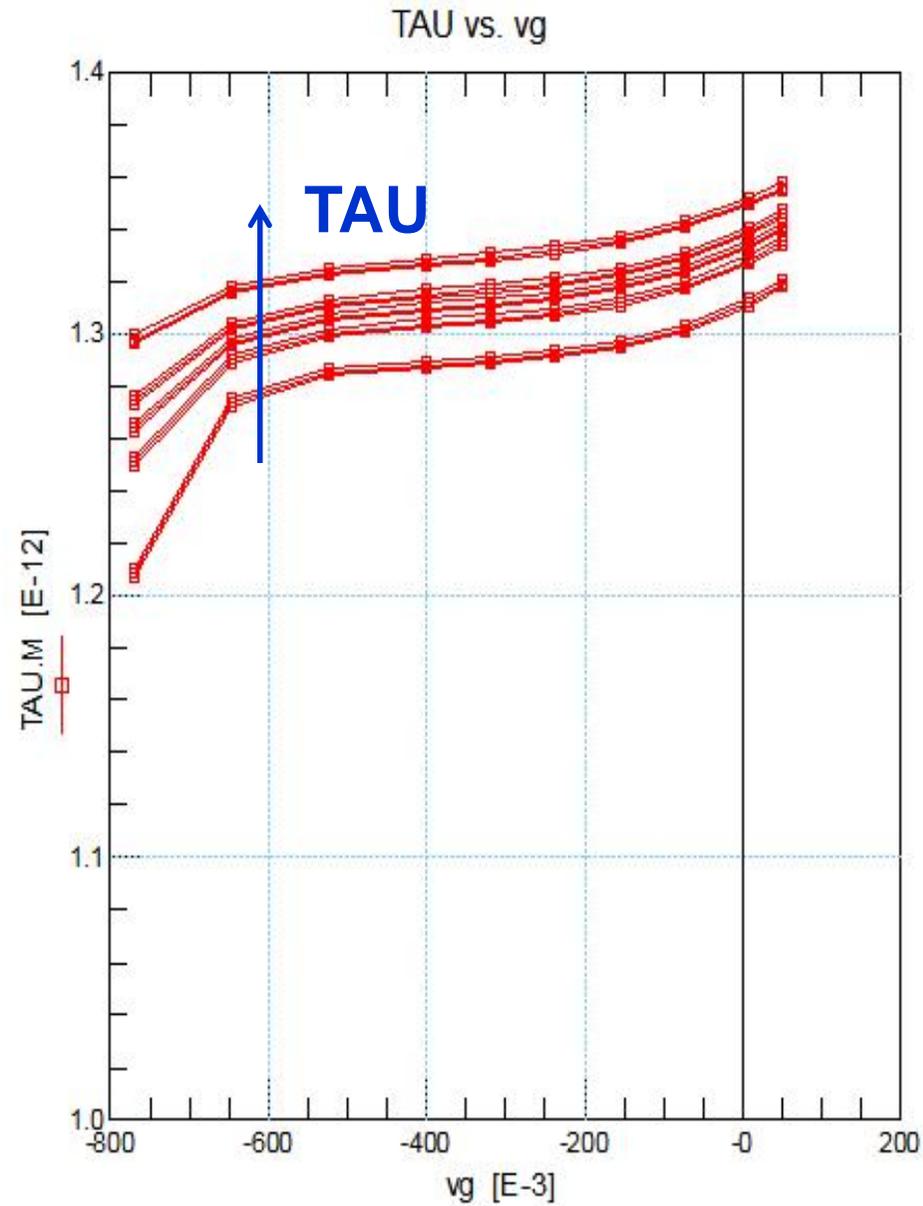
CGD

@ vd 1st sweep
vg 2nd sweep



TAU

@ v_g 1st sweep
vd 2nd sweep



Outline

- Introduction to the Angelov Model

- **Step-by-Step Modeling Sequence**

 - Resistances R_G , R_D , R_S

 - DC Input Characteristic i_g - v_{gs}

 - DC Transfer Characteristic i_d - v_{gs}

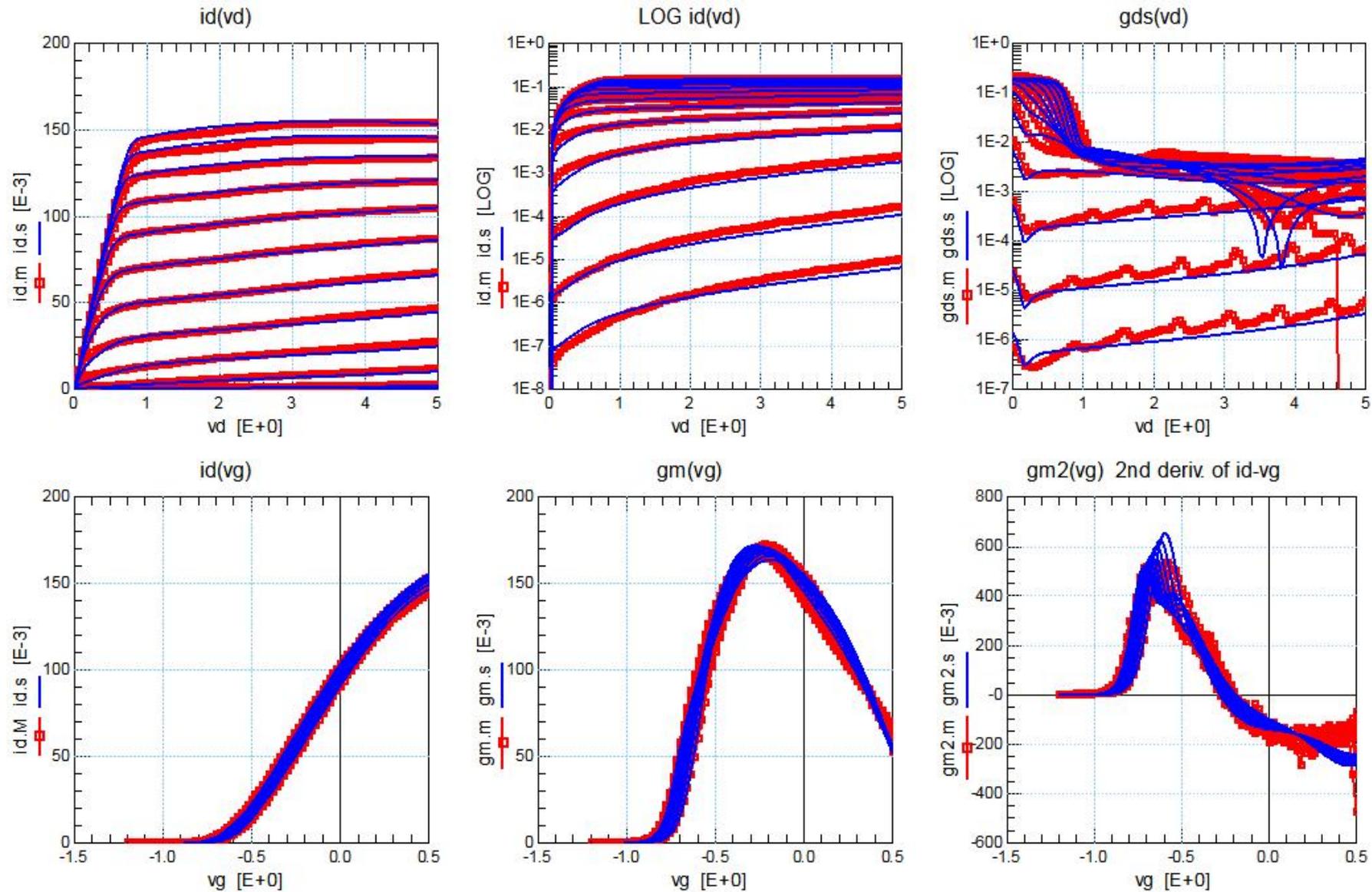
 - DC Output Characteristic i_d - v_{ds}

 - Thermal Modeling

 - S-Parameter Modeling

- **Modeling Results**

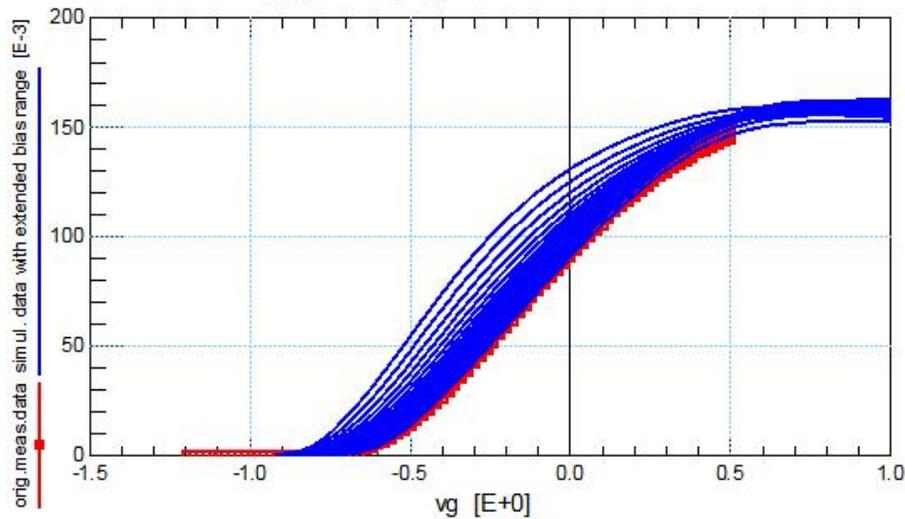
DC Modeling Result



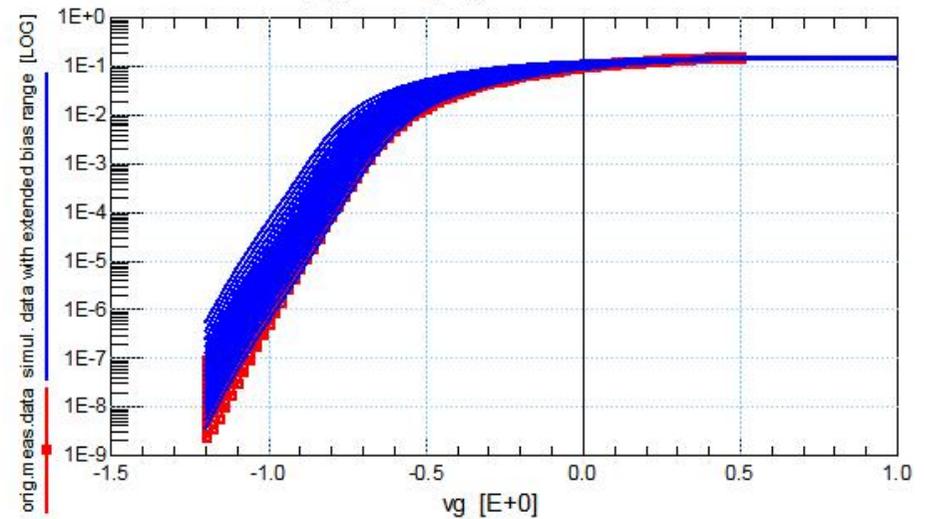
Model Robustness Check

measurements
extended simulation range

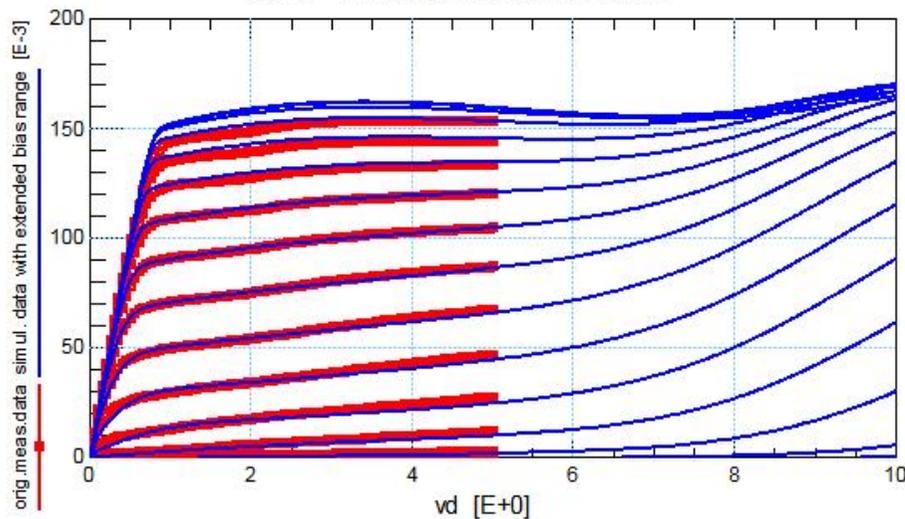
id_vg: Verifying Model Robustness



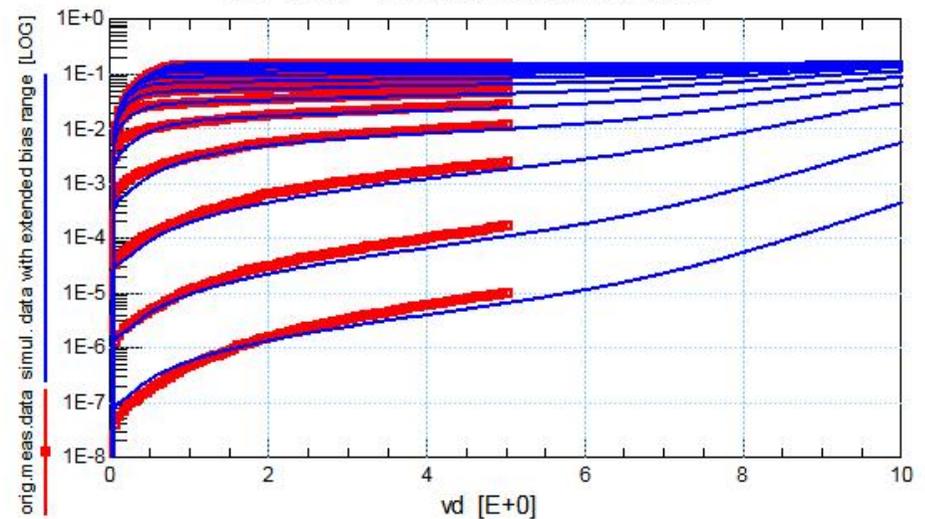
LOG id(vg): Verifying Model Robustness



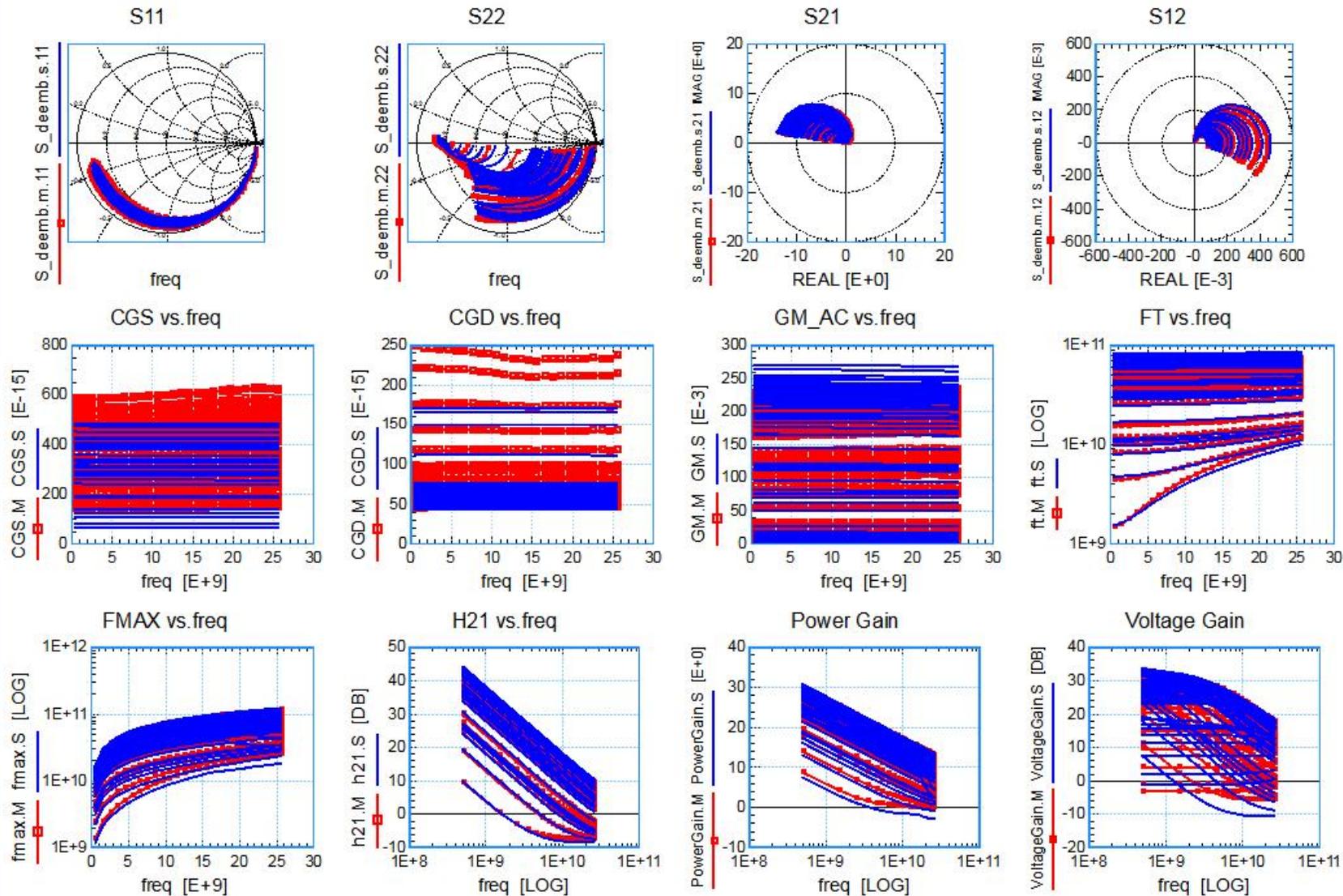
id_vd: Verifying Model Robustness



LOG id(vd): Verifying Model Robustness



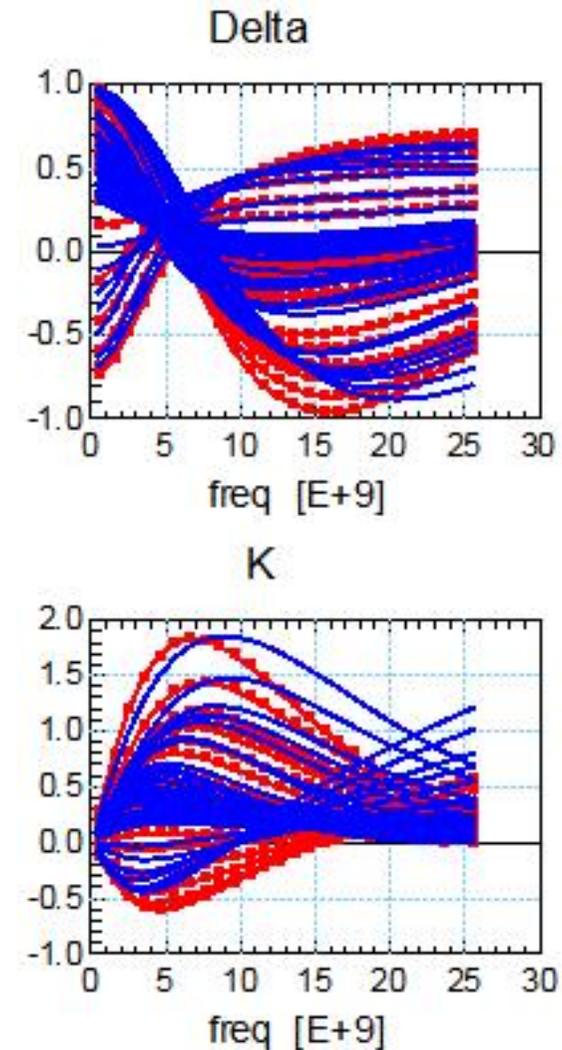
S-Parameter Modeling Result



Stability K-Factor Check

$$\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{21} \cdot S_{12}|}$$



The Stability Factor K, together with its determinant Δ part, are a good measure to check the fitting of simulated to measure data of all four S-parameters, in a single plot.



Dr.-Ing. Franz Sischka

**Consulting Services
for Electronic Device
Measurements,
Data Verification
and Modeling**

www.SisConsult.de

eMail: franz.sischka@SisConsult.de