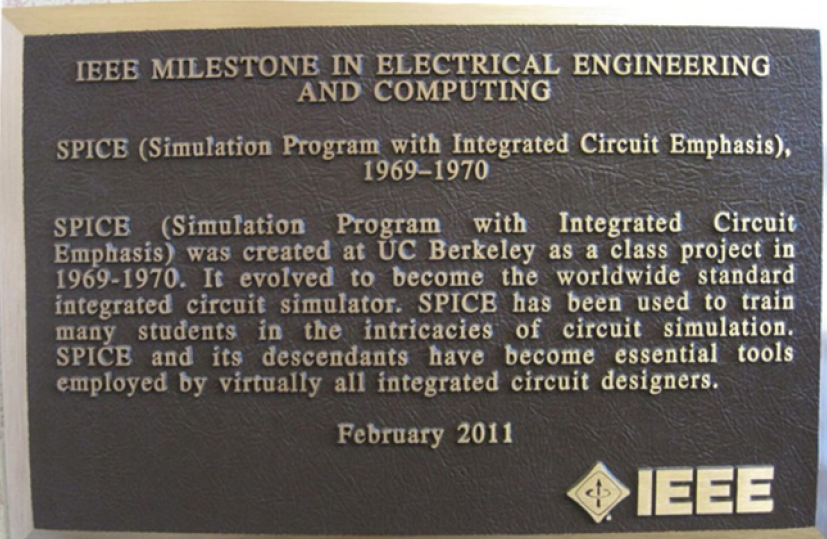


What is a Spice Model Card ?

SPICE




IEEE MILESTONE IN ELECTRICAL ENGINEERING AND COMPUTING


SPICE (Simulation Program with Integrated Circuit Emphasis), 1969-1970

SPICE (Simulation Program with Integrated Circuit Emphasis) was created at UC Berkeley as a class project in 1969-1970. It evolved to become the worldwide standard integrated circuit simulator. SPICE has been used to train many students in the intricacies of circuit simulation. SPICE and its descendants have become essential tools employed by virtually all integrated circuit designers.


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SPICE (Simulation Program with Integrated Circuit Emphasis) is a standard tool for circuit designers to simulate and predict the behavior of integrated circuits, before they are manufactured. Once manufactured, the circuits are measured and compared to the previous simulations.

A prerequisite for this flow is to have accurate and valid device models available, from which the designer composes his circuit.

The term 'with Integrated Circuit Emphasis' in the naming of Spice is an indication to the smart concept of the model implementation for integrated circuits (ICs):

- many transistors or diodes based on the same production process, but possibly different in size (for different current flow requirements)
- these many transistors/diodes with their individual connection nodes and geometry information, each link to the same model description (formulas) with the basic model parameters, which are valid for the geometrically normalized device size.

SPICE has been developed in the early 1970's at UC Berkeley/California by Laurence Nagel, to assist with teaching electronic circuit design to students . At that time, it was about 6000 lines of FORTRAN program code.

A Perspective on Computing in the '70s

- The computer at UC Berkeley in the '70s was a CDC 6400
- The input to the computer was punched cards
- The output of the computer was a line printer
- The MIPS rate was comparable to an Intel 286 (1 MIPS)
- The maximum available memory was 100,000 octal 60 bit words daytime and 140,000 octal at night (comparable to 256 KByte)

Slide from MOS-AK Athens, Sept.2009:
Laurence Nagel* and Colin McAndrew**, "SPICE and Models - Perfect Together"
*Omega Enterprises Consulting; **Freescale Semiconductor



It became popular because of its simple and efficient netlist syntax, the implemented models (Diode, Gummel-Poon bipolar model) and its availability as a public domain software.

Why SPICE Was Successful

- It contained simple built-in models for BJTs, diodes, JFETs, and MOSFETs (thanks to Dave Hodges)
- It was fairly easy to use (some classmates may disagree)
- It was readily available and in the public domain
- At 8,000 lines of FORTRAN, students could make modifications to fit special needs
- Students could take SPICE with them to their new job

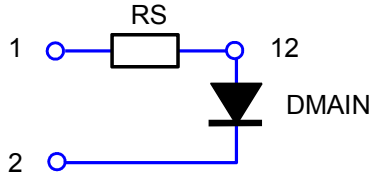
Slide from MOS-AK Graz, Sept.2015:
Larry Nagel, "Is SPICE Still an Educational Tool?"
Omega Enterprises Consulting




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Let us discuss a simple netlist, consisting of a diode in series with a resistor, as shown below:

Diode Spice Netlist



```
.SUBCKT myDiode 1 2
RS 1 12 2.5
DMAIN 12 2 MAIN
.MODEL MAIN D IS=1E-18 N=1 CJO=1p VJ=0.6 M=5 FC=5 TT=1f BV=100 IBV=1m KF=0 AF=1 XTI=3 EG=1.11
.ENDS
```



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The beauty of a SPICE netlist is its clear and simple structure:

for every electronic device, a line needs to be defined, beginning with a key character for the component (e.g. R for a resistor, C a capacitor, L an inductor, D a diode, Q a transistor), followed by the user-defined component name. Then come the nodes, and finally the device parameter value.

Example for a 2.5 Ohm resistor between nodes 1 and 12:

```
Rmyname 1 12 2.5
```

Diodes and transistors are usually described by two components:

- first the so-called instance, i.e. the key-character and the user-name, the nodes, and finally a link keyword to a 'model card'.

- the other line of code, the 'model card', starts with the keyword '.MODEL', followed by the previous mentioned keyword of the device instance, the link to the SPICE-internal model equations ('D' for diode model), and the model parameters (the specific parameter values for the SPICE model equations).

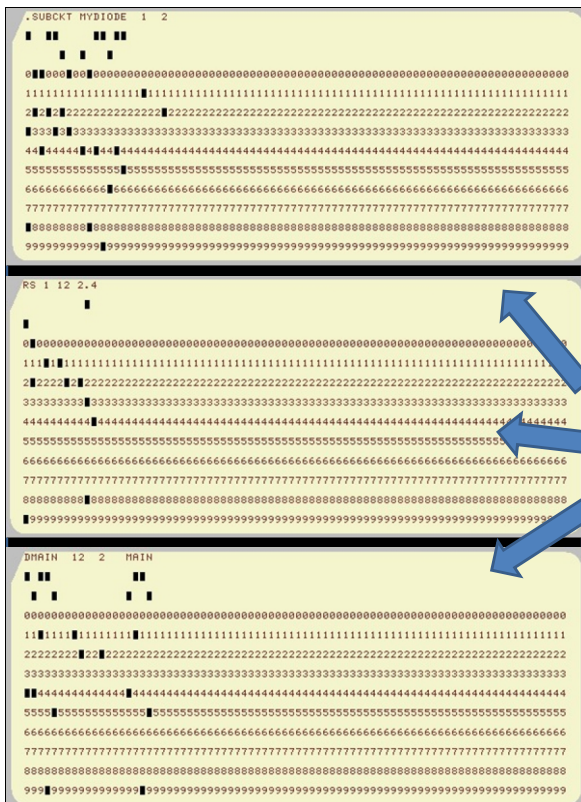
This idea of an instance line (connections) and a model line (description of the electrical performance) is a key usability factor for the design of integrated circuits, where many identical components are used at different locations in the circuit netlist.

The 1970's were the time of programming computers using punch cards. Every line of code was represented by an individual punch card.

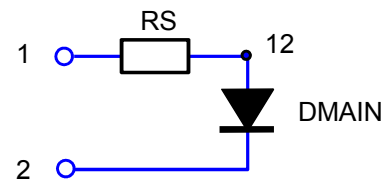
Punch Card Writer



Below, the punch cards for the first 3 lines of our SPICE netlist example:



Punch Cards for Spice Netlists



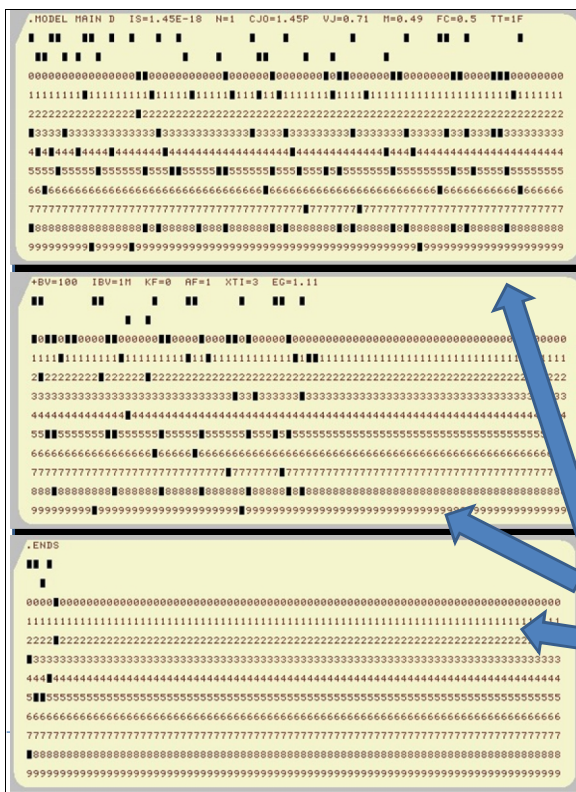
```
.SUBCKT myDiode 1 2
RS 1 12 2.5
DMAIN 12 2 MAIN

.MODEL MAIN D IS=1E-18 N=1 CJO=1p VJ=0.6 M=.5 FC=.5 TT=1f
+BV=100 IBV=1m KF=0 AF=1 XTI=3 EG=1.11

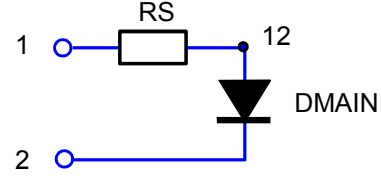
.ENDS
```

Consequently, the next line, hosting the .MODEL description was also represented by a punch card: **the so-called Model Card**.

If the .MODEL line was longer than what fits on a punch card, a 2nd card was applied, starting with the key character '+', as in our example:



Punch Cards for Spice Netlists (cont'd)



```
.SUBCKT myDiode 1 2
RS 1 12 2.5
DMAIN 12 2 MAIN

.MODEL MAIN D IS=1E-18 N=1 CJO=1p VJ=0.6 M=.5 FC=.5 TT=1f
+BV=100 IBV=1m KF=0 AF=1 XTI=3 EG=1.11

.ENDS
```

The Model Card

The next slide depicts the simulation request for a DC current characteristics of a diode, with the anode voltage from 0V -> 1V, and cathode grounded.

The Spice Input Deck

User Netlist

```
.SUBCKT SPICE_DIODE 1 2
RS 1 12 2.4
DMAIN 12 2 MAIN

*MODEL CARD
.MODEL MAIN D IS=1.45E-18 N=1 CJO=1.45p VJ=0.71 M=0.49 FC=0.5 TT=1f
+BV=100 IBV=1m KF=0 AF=1 XTI=3 EG=1.11

.ENDS
```

Simulation Request

```
* SUBCKT CALL
XCKT 1 2 SPICE_DIODE

* START SOURCES
VAGRO 1 0 DC 0
VCGRO 2 0 DC 0
* END SOURCES

* SIMULATION TEMPERATURE
TEMP 27

* SIMULATION REQUESTS
.DC VAGRO 0.1 1 0.02
.PRINT DC I(VCGRO)
.PLOT DC I(VCGRO)

.END
```

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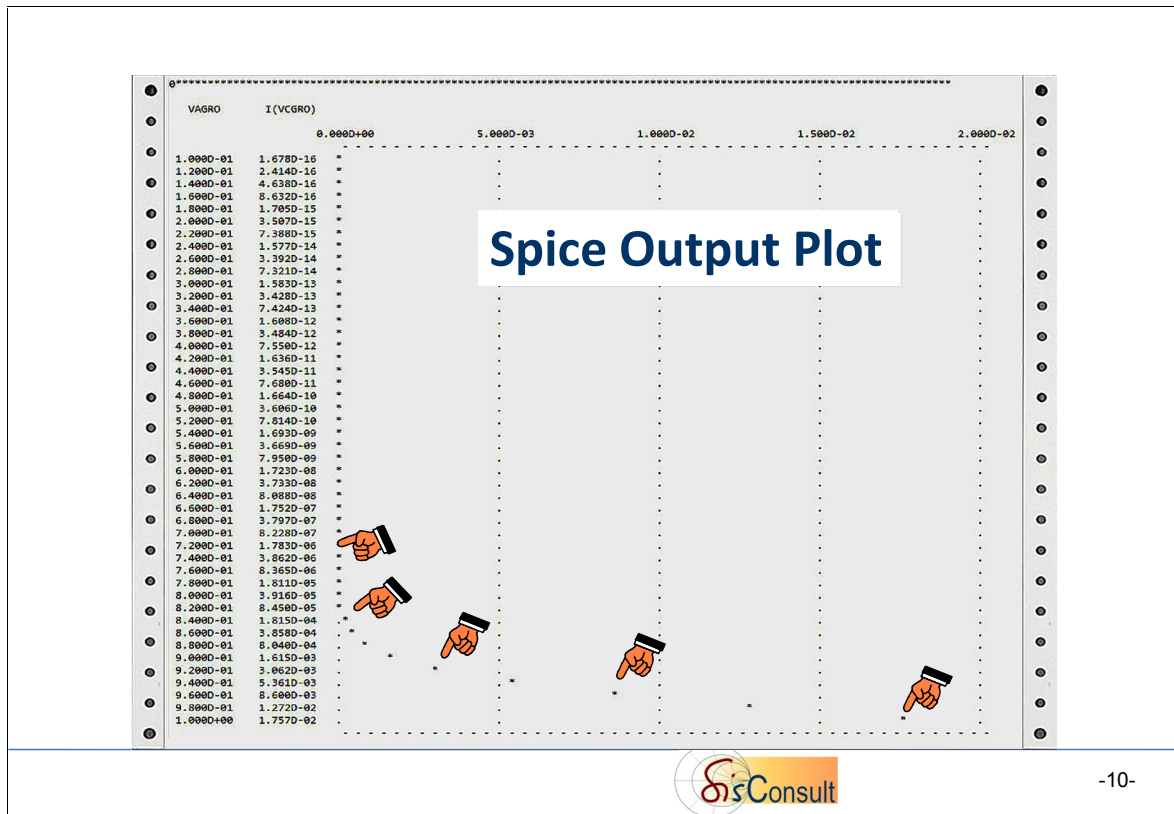
And the resulting Spice output was then printed in data columns on endless computer paper like this:

VAGRO	I(VCGRO)
1.0000e-01	1.6780e-16
1.2000e-01	2.4040e-16
1.4000e-01	4.6330e-16
1.6000e-01	8.6320e-16
1.8000e-01	1.7090e-15
2.0000e-01	3.3070e-15
2.2000e-01	7.3000e-15
2.4000e-01	1.5770e-14
2.6000e-01	3.3920e-14
2.8000e-01	7.3210e-14
3.0000e-01	1.5030e-13
3.2000e-01	3.4290e-13
3.4000e-01	7.4240e-13
3.6000e-01	1.6000e-12
3.8000e-01	3.4040e-12
4.0000e-01	7.3590e-12
4.2000e-01	1.6360e-11
4.4000e-01	3.5450e-11
4.6000e-01	7.6090e-11
4.8000e-01	1.6060e-10
5.0000e-01	3.6060e-10
5.2000e-01	7.8040e-10
5.4000e-01	1.6930e-09
5.6000e-01	3.6090e-09
5.8000e-01	7.9500e-09
6.0000e-01	1.7230e-08
6.2000e-01	3.7330e-08
6.4000e-01	8.0000e-08
6.6000e-01	1.7520e-07
6.8000e-01	3.7970e-07
7.0000e-01	8.2200e-07
7.2000e-01	1.7600e-06
7.4000e-01	3.8020e-06
7.6000e-01	8.3020e-06
7.8000e-01	1.8110e-05
8.0000e-01	3.9050e-05
8.2000e-01	8.4500e-05
8.4000e-01	1.8150e-04
8.6000e-01	3.8500e-04
8.8000e-01	8.0400e-04
9.0000e-01	1.8150e-03
9.2000e-01	3.8020e-03
9.4000e-01	8.3010e-03
9.6000e-01	1.8000e-02
9.8000e-01	3.7220e-02
1.0000e+00	8.1750e-02

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Using a so-called 'chain printer', "plotting" was using ASCII characters for x-y charts.



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