TUTORIAL ABOUT ELECTRONIC DEVICE MODELING

This tutorial explains the basics of electronic device modeling,
by the example of

MODELING OF A SOLAR-POWERED LED ARRAY

Keywords:

Solar Powered, Circuit Development, Device Modeling, Solar Cell, Accumulator, Diode, LED, Transistor

Contents

March 2014
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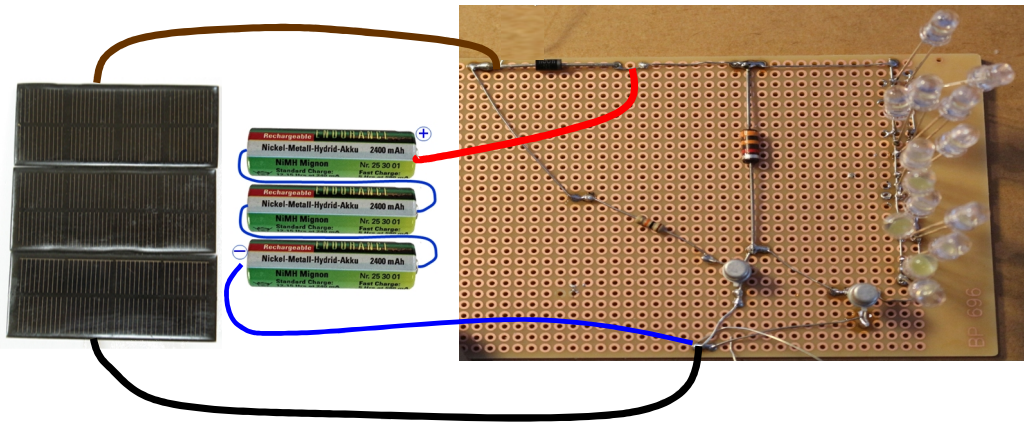
Solar-Powered LEDs

A Tutorial Device Modeling Example

- not only for modeling engineers -



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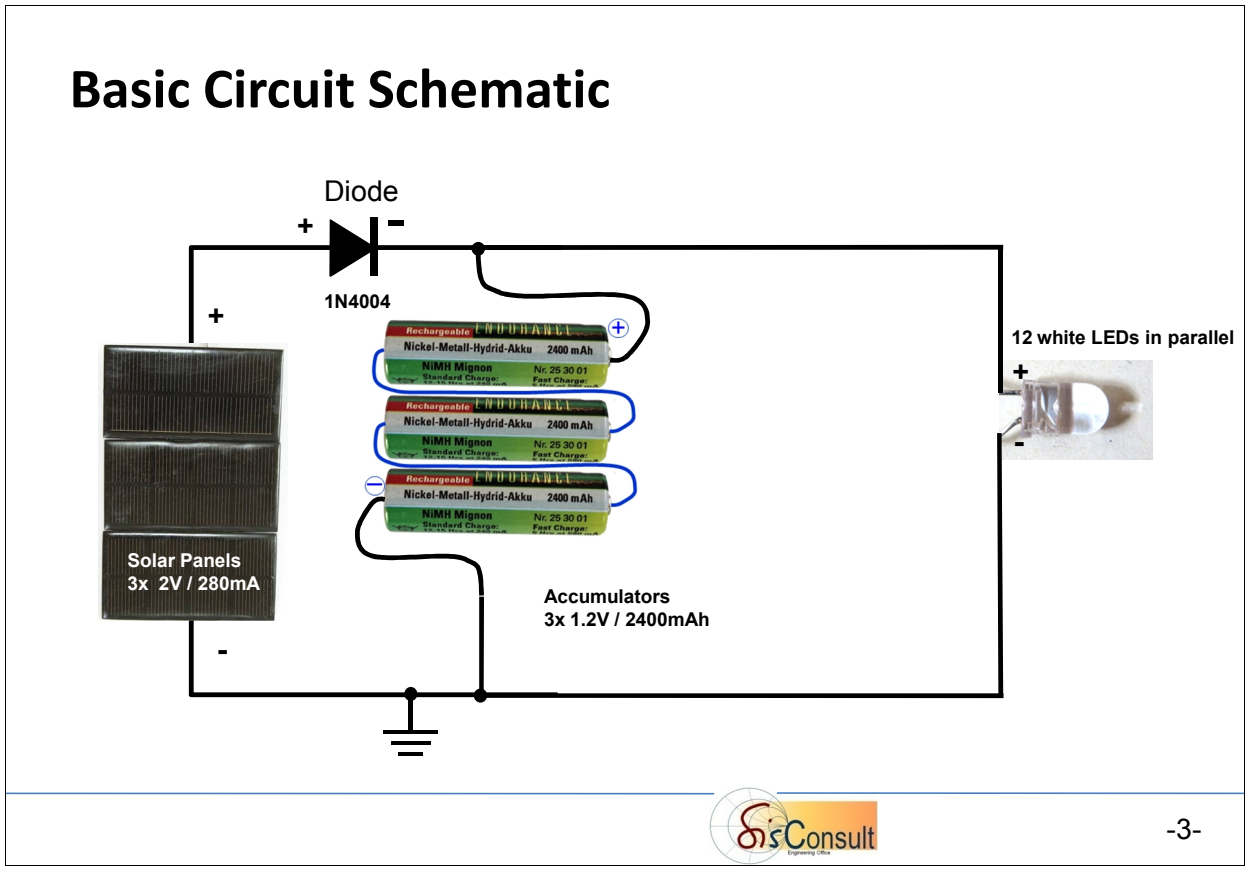
The goal of this tutorial is to

- first develop an electronic circuit schematic for an array of solar-powered LEDs:
  During sun light, the accumulator shall be charged, and during night time, the accumulator shall power the LEDs.
- In a second step, Spice Models for each component of the schematic will be developed.

This will enable to simulate the performance of the complete circuit.
If the models have been developed accurately, the simulation result will match the built-up and measured circuit.

The outcome of the tutorial: the use of models in simulation allows to develop, fine-tune or optimize the circuit without the need for building it up. Therefore, modifications due to new components (other accumulators, solar cells or LEDs) can be evaluated easily on a computer. This scenario corresponds to today's chip development and fabrication: a circuit, fulfilling the requirements of a certain functionality, is developed by Spice simulations on a computer. The chip is then fabricated by a wafer fab, packaged and used as a complete function block IC (Integrated Circuit) on a PC board (Printed Circuit Board).

The Development of the Circuit Schematic

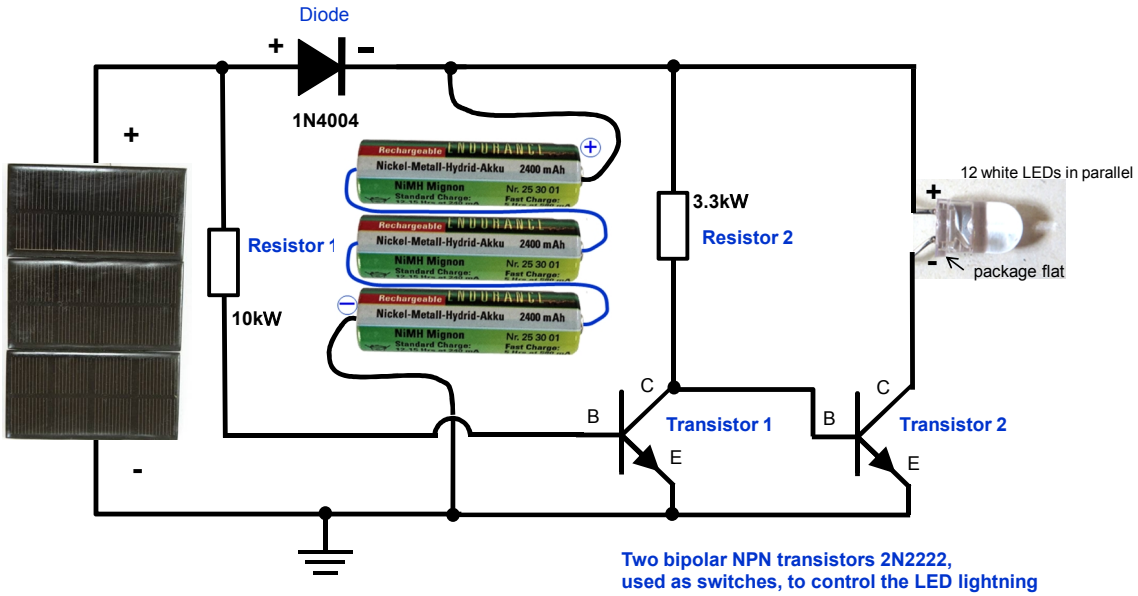


The basic circuit consists of 3 solar panels (2V/280mA peak each), connected in series, followed by a diode to charge the 3 accumulators (e.g. Nickel Metal Hydride Accumulators, 1.2V/2500mAh each), which are connected in series.
The reason for the diode is to prevent reverse current flow from the accumulators through the panels during night time.

Finally, in parallel to the accumulators are 12 white LEDs, which feature a good light emission at a voltage of ~3.6V, what corresponds perfectly the accumulator chain's voltage.

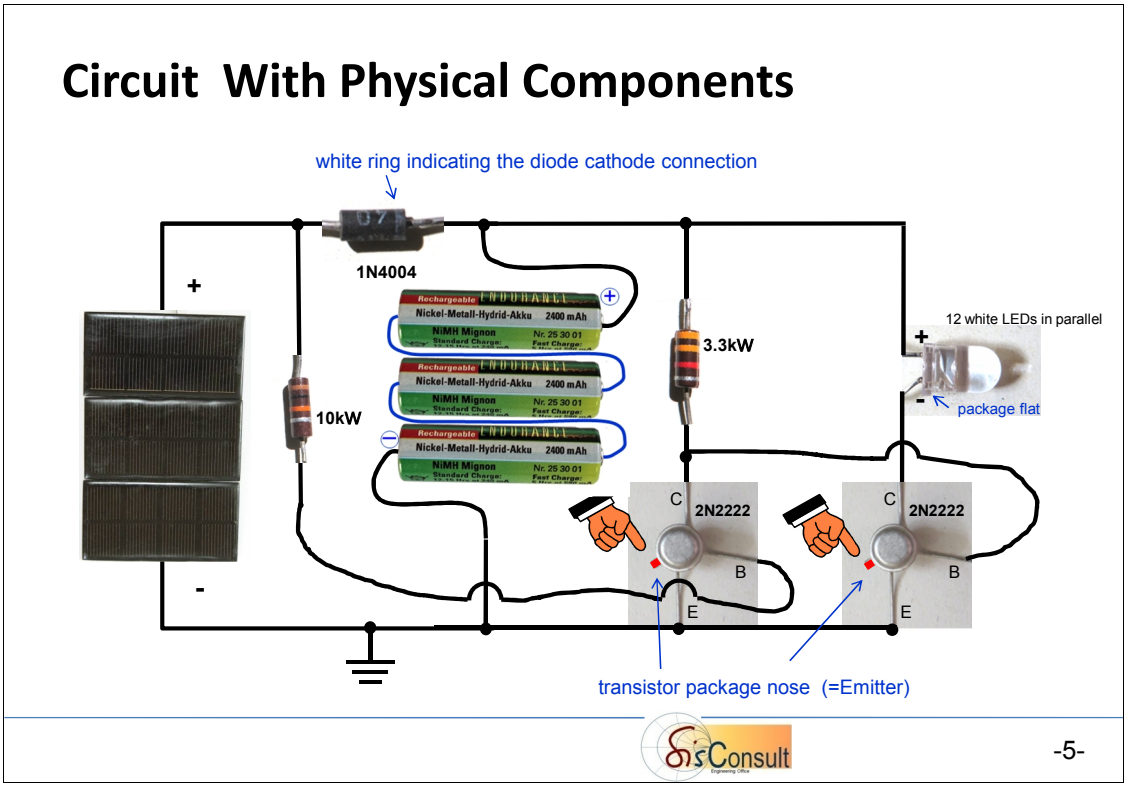
However, the LEDs are also lighting during the day-light's accumulator charging.
Adding a simple switching circuit, as depicted below, will prevent this.

Final Circuit Schematic



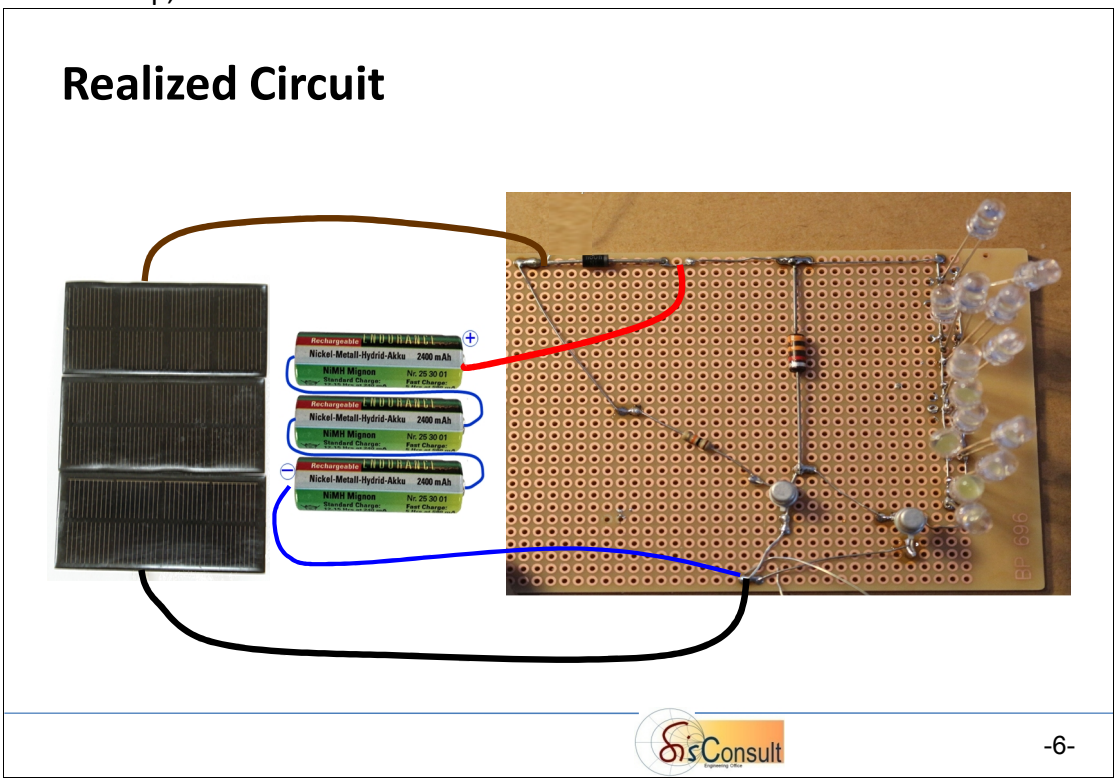
The desired circuit functionality is to switch-on the LEDs only during night time.

- the LEDs are no longer connected directly to the accumulators, but instead, a transistor (Transistor 2) is inserted. This Transistor2 will behave like an on-switch, if its control pin, the Base 'B', is powered by ~0.75V or more. This is provided by Resistor2. Transistor2 and Resistor2 alone, however, will always switch-on the current through the LEDs, but they now offer the ability to switch the LEDs on or off.
- This switching is achieved by Resistor1 and Transistor1: If the solar panel is providing current and charges the accumulators, there will be a current through Resistor1, into the Base(B)-Emitter(E)-junction of the Transistor1, what will make its Collector(C)-Emitter(E) pins behave like a short circuit. Consequently, Transistor2 is no longer conducting, and so, the LEDs will be switched off.
- In the opposite case, during night time, no current will be provided by the solar panel, and no current will flow into the Base 'B' of Transistor1. Its Collector-Emitter junction is switched-off, behaves like an open. This enables the current through Resistor2 to flow into the Base of Transistor2, switching its Collector-Emitter junction on, and therefore, enabling current flow through the LEDs, emitting white light.



The above slide covers the same schematic as before, but for the reader's convenience, showing this time the physical components before soldering them on a connection board.
Just in case you want to build up this circuit by yourself ...

And here is the built-up, soldered circuit.



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The Modeling of the Circuit Components

The story behind the previous slides covered the state-of-the-art of electronic circuit design with lumped, individual components: developing a circuit schematic, and building it up by soldering electrical components together.
If there is need for modification, because a different solar panel should be used, or other transistors etc., the components can easily be un-soldered and replaced by other ones. Also, optimizing of component values (here, for instance the resistor values), can be achieved easily by un-soldering the old ones and soldering the new ones.

However, when thinking of integrated circuits (ICs), also called chips, this method does not work anymore, because all the applied components (Diode, Resistor1, Resistor2, Transistor1 and Transistor2) are integrated into the chip (physically onto the surface of a piece of a crystal), and cannot be replaced or modified any more. Therefore, no try-and-error to adjust the components is possible any more. In other words, the very first production of such a crystal (chip) must result in a 100% performance, as desired by the design engineer.

This can be achieved when mathematical models exist for each electrical component. These models, i.e. mathematic formulas, describe the current-voltage behavior of each component accurately, and instead of physical soldering of lumped components, these formulas are concatenated in a mathematical solver program, and provide a simulation result of the complete crystal-to-be-produced.

An example of such a program is Spice (Simulation Program with Integrated Circuit Emphasis), developed already in the early 1970ies at the University of California, Berkeley, and their today's counterparts like PSpice, LTSpice, HSpice, Spectre, ADS etc..

In the next slides, we will develop simple models for the used components, which will finally enable the simulation of the whole circuit.

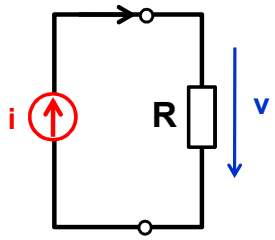
We will begin with the simplest model, for a resistor, and end with the most complex, the bipolar transistor.

Modeling the Resistors

Resistor Model Equation

$$R = \frac{v}{i}$$

The Measurement Setup:



The general SPICE Resistor Model Card Definition is:

```
R_myname   +Node  -Node    R_value
```

and for our two resistors:

```
R1    +Node   -Node    10k
R2    +Node   -Node    3.3k
```

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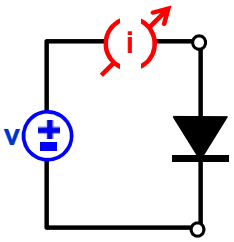
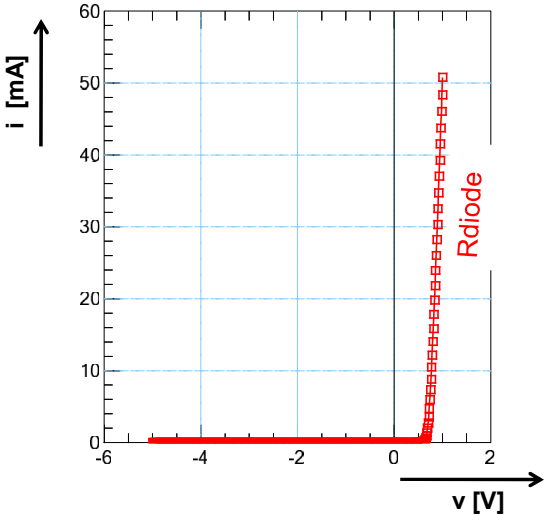
Modeling a resistor is pretty straight-forward:
a test current is fed into the resistor and the voltage drop across the resistor pins is measured.
Following the Ohmic law, its resistance R is **R=v/i**.
And this is at the same time already the model of the resistor.

Diode Modeling
- some preconsiderations-

The Measurement Setup:



Measured Diode Characteristics:



For negative bias voltage, the diode current is zero (infinite resistance),
while for a positive bias voltage, above a certain threshold (typ. 0.7V for silicon),
the diode becomes conductive, with a resistance Rdiode

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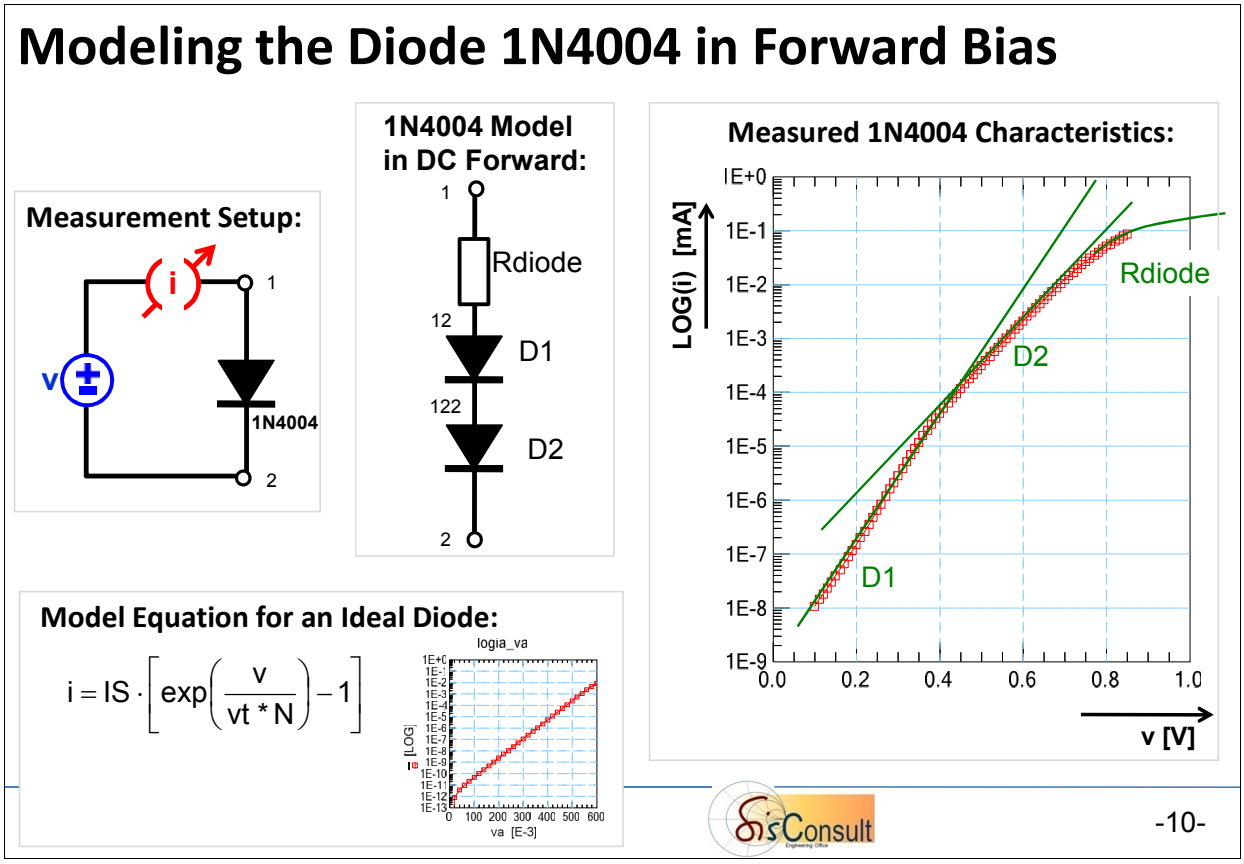


For a better resolution of the below-threshold state, the diode measurement result (above, on the right) is shown in a semi-logarithmic plot:
- the current 'i' on the y-axis, ranging from nano-Ampere to ~100mA, is drawn in a LOG_{10} scale,
- while the stimulating voltage 'v' is in linear scale.

The equation of the *ideal* diode model, in forward bias, is given above on the lower left, and displayed also by a semi-logarithmic plot: it's a single, straight line, where

- the diode model parameter 'IS ' represents the y-intercept,
- while the other diode parameter 'N' models the slope, together with the so-called temperature voltage 'vt' (27mV @ 27°C).

However, the measurement result of the diode 1N4004, above on the right, clearly shows <u>*two*</u> such linear regions, followed by a declining curve at high bias 'v'.
This declining curve at highest DC bias represents the ohmic resistance of the diode in on-state (in a lin/lin scaling plot, it would be represented by a straight line, as depicted already before, in the last-but-one slide).

The two straight line segments below the threshold voltage can be modeled <u>*each*</u> by a combination of two mentioned *ideal* diode models:

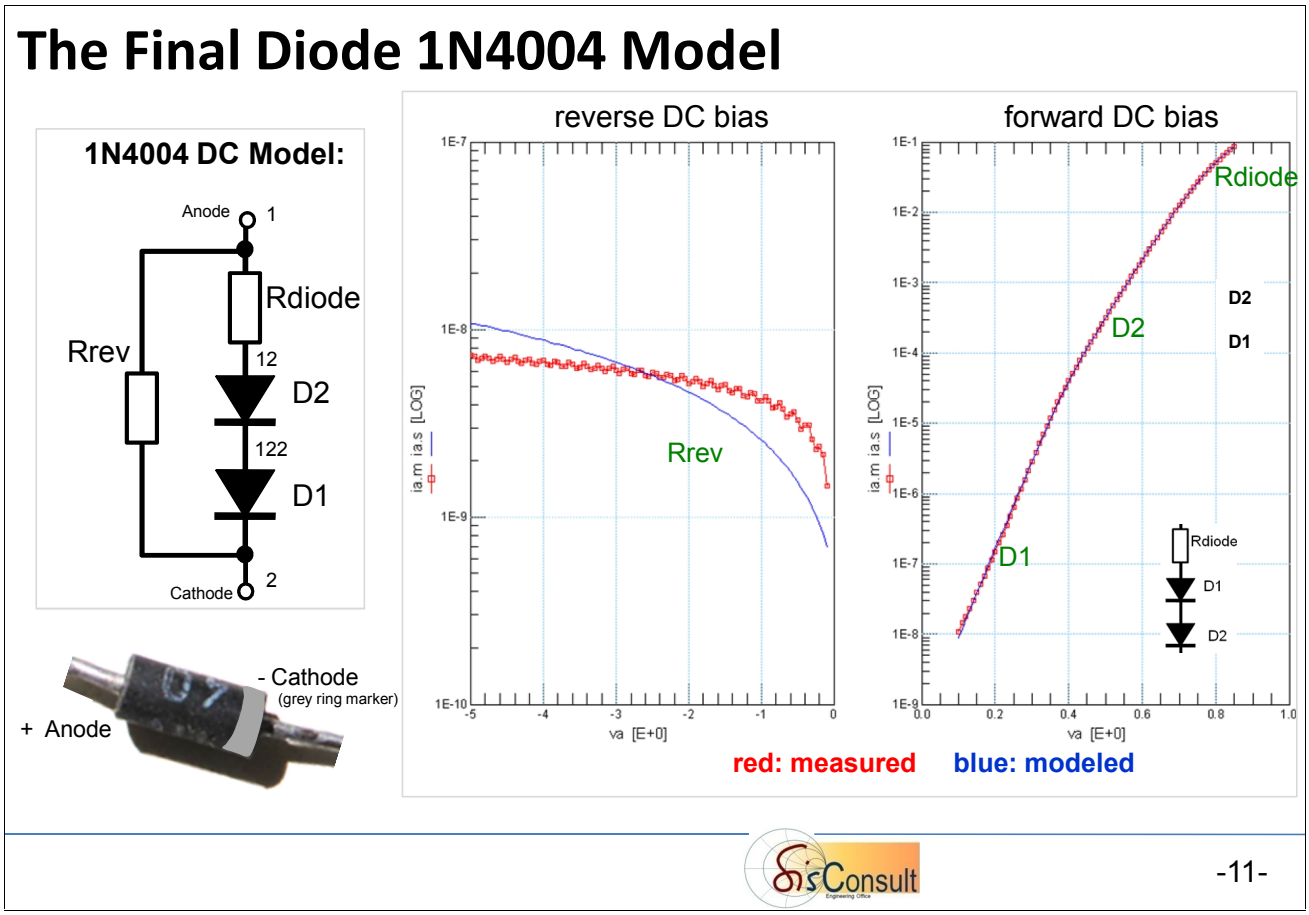
- The ideal diode model 'D1', between simulation nodes '12' and '122', fits the measurement up to v~0.4V. The y-intercept of this measurement segment corresponds to the model parameter D1.IS, and the slope corresponds to D1.N.
- Above v~0.4V, 'D1' predicts too much current 'i' for a given diode voltage 'v'. But this scenario can also be interpreted the other way: at a given diode current 'i', there is more voltage drop 'v' than predicted by diode model 'D1'. This additional voltage drop is modeled by the second ideal diode model 'D2', which is ***<u>in series</u>*** with 'D1' (between the simulation nodes '122' and '2').

Model parameter extraction for diode 'D2':
Continuing the interpretation of our modeling problem by a forcing diode current, there is no voltage drop across the diode unless the forcing current is larger than model parameter 'IS'. This means: The current at the take-over point of the 'D2' diode (~5E-5A) corresponds to the model parameter D2.IS, and the slope of the second line is modeled by parameter to D2.N.

- Finally, above v~0.7V, another additional voltage drop happens for currents predicted this time by 'D2'. This is covered by the already mentioned series resistor 'Rdiode', between the simulation nodes '1' and '12'.

The resulting sub-circuit model for the forward biased 1N4004 diode is shown in the middle of the above slide.

For reverse voltage bias, the ideal SPICE diode model predicts an ideal, voltage-independent leakage current 'I_leakage', which is I_leakage = -IS. In practice, however, this is most often not quite the case.



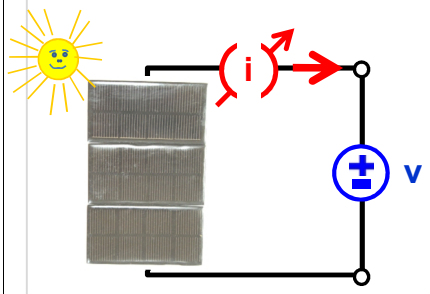
In our case, for the 1N4004 DC reverse current measurement, down to v = -5V, we obtain roughly -8nA (see the plot in the center of the above slide). Because this reverse current is so small, we could ignore it and stay with the previous forward diode model.
But, to demonstrate device sub-circuit modeling further, we improve our Spice model by a resistor 'Rrev'.
Note: Its value is so large, that it does not affect the model performance in forward bias range.
The resulting fitting, shown above (measurement: red, modeled: blue), is fully sufficient for our application.

The netlist of the resulting, complete 1N4004 diode model is (in SPICE syntax):

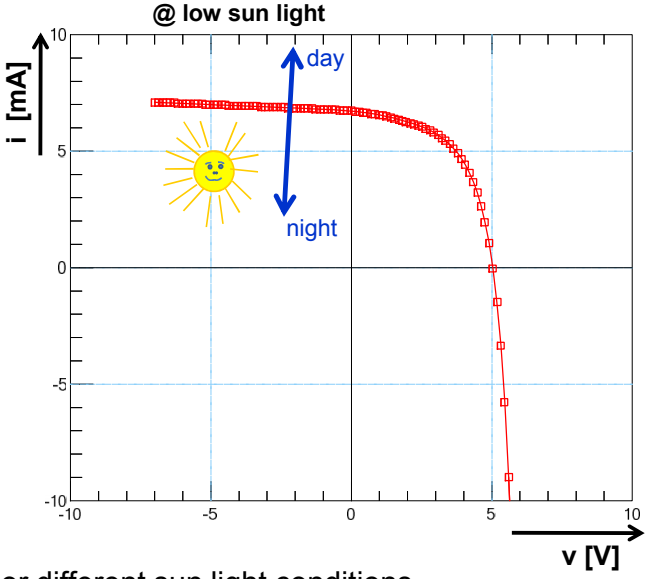
```
*                     1=Anode 2=Cathode
.SUBCKT diode_1N4004  1       2
*model instances forward bias
Rdiode   1   12  0.631
Dhigh   12  122  D2
Dlow   122    2  D1
*model instances reverse bias
Rrev     1    2  4.73E+08
*model cards
.MODEL D1   IS = 5.15E-10 N = 1.338
.MODEL D2   IS = 5.05E-05 N = 0.727

.ENDS
```

Measuring the Solar Cells

The Measurement Setup:



Measured Solar Cell Characteristics
@ low sun light



For different sun light conditions,
the load voltage 'v' is varied,
and the current 'i' out of the solar cell is measured.

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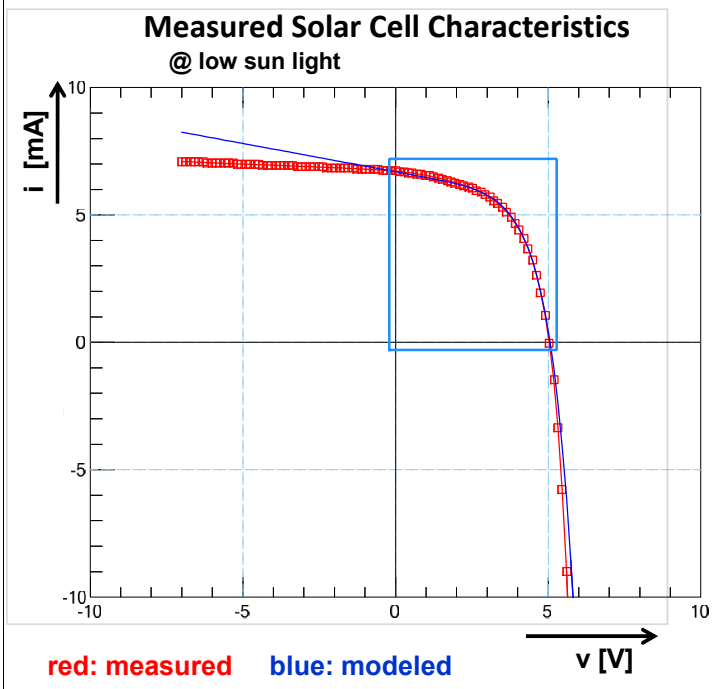
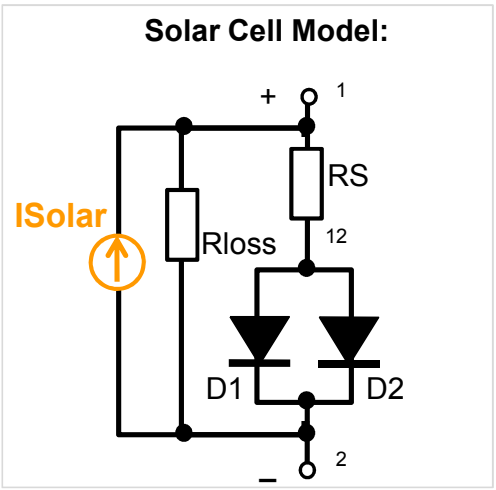
For the measurement of the solar cell at low sun light, we apply a voltage sweep 'v', which emulates the dissipation of the load attached later to the solar cell:

- When the applied v = 0V, the emulated load is a SHORT (i.e. the accumulator is completely empty and will be loaded by maximum available (solar-generated) current)
- and when v > 0V and the solar cell current is zero, the load (i.e. the accumulator) is fully charged.

For the modeling of the solar cells, the important region is the bias voltage between v = 0V (solar cell is shorted - max. current) and the voltage for which the solar cell current becomes zero (accumulator is charged). See the blue box in the plot below.

Modeling the Solar Cells

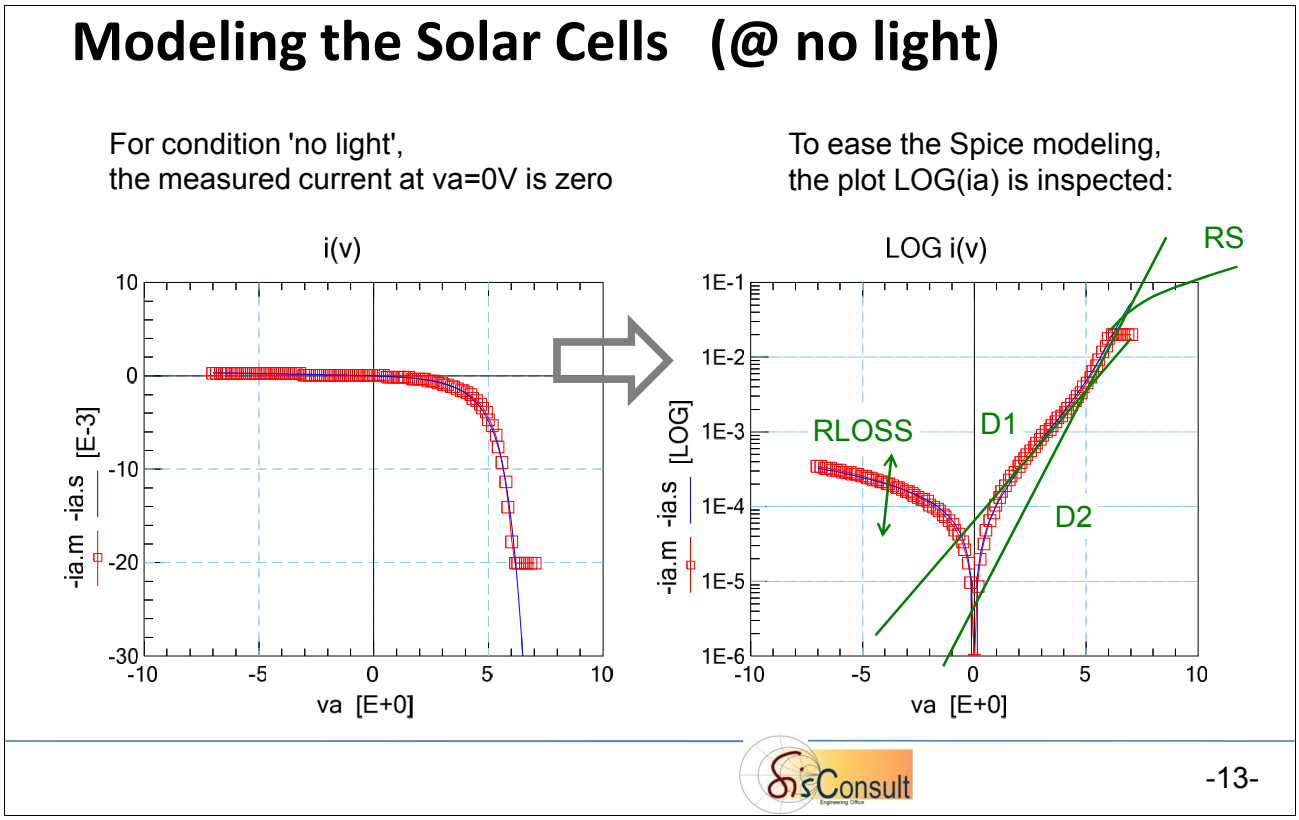




Developing the model:

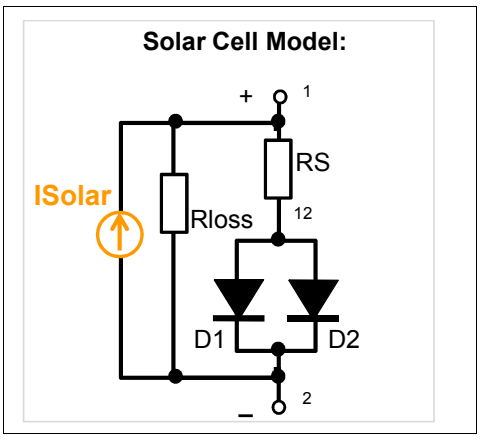
- The current at v = 0V is proportional to the solar light, modeled by an ideal current source 'ISolar' (see above, on the right).
  → the more sun light, the more 'ISolar'.
- The slight slope at v ~ 0 is modeled by resistor 'Rloss', in parallel to 'ISolar'.
- The decline of current for v > 0 until v(i = 0) can be modeled by a diode 'D1', in series with a resistor 'RS'.

For a more detailed Spice model development, we begin with the case 'no sun light', as shown below.
On the left the measurement result in linear scale, and on the right the same in semi-logarithmic:

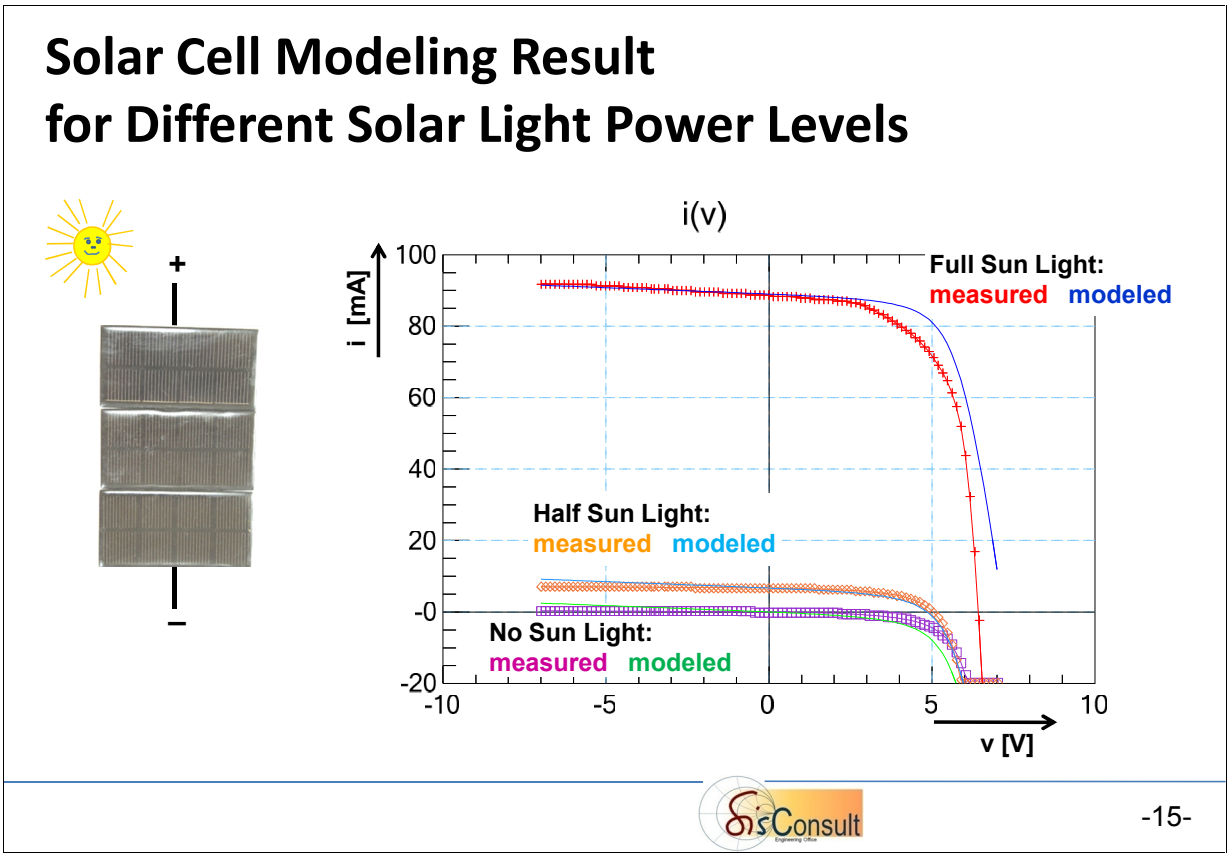


Following best-practice modeling, we go from left (lowest va) to right (highest va) on the plot above, on the right:

- for va < 0V, tuning RLOSS provides a good fit
- above 0V, diode D1 models the trace well until ~5V.
- above 5V, the measured current is higher than predicted so far by simulation:
  - more current at the same voltage means: add a component in parallel
  - since the trace is again linear in the semi-log plot, we go for a diode D2, *in parallel* to D1
- for completeness, we also add a series resistor RS to the sub-circuit model.

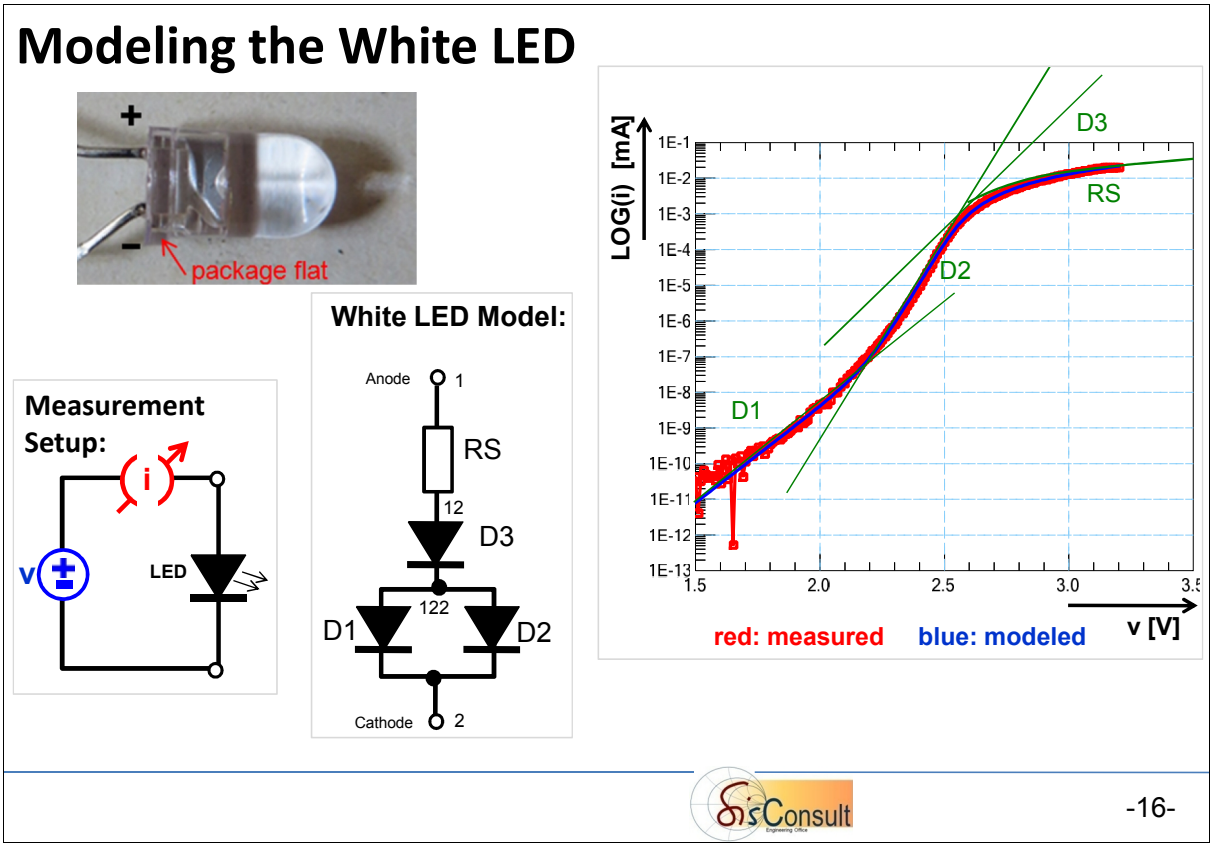


The next slide depicts the modeling result for various sun light levels:



The netlist of the resulting solar cell model finally is (in SPICE syntax):

```
*                       1=Plus     2=Minus
.SUBCKT   solar_cell    1          2

ISolar 2 1 0     * varies with light

*model instances
Rloss 1   2   2.869k
RS     1 12   10.91
D1    12   2   D1
D2    12   2   D2

*model cards
.MODEL D1 D   IS = 4.161E-005   N = 41.33
.MODEL D2 D   IS = 2.801E-009   N = 14.15

.ENDS
```



Like with the previous modeling of the 1N4044 diode, we apply again a sub-circuit model for electronic performance of the White LED.
And, once again, the model development is determined by the measurement result:

- Applying a semi-logarithmic plot, three regions of straight lines can be identified:
  -> two regions of straight lines, represented in the model by diodes 'D1' and 'D2'
  -> and the region of ohmic effects with a declining curve at highest bias voltage: resistor 'RS'

As in the examples before, the modeling starts at the lowest applied bias, and continues with modeling the incrementing bias regions of the measurement: in the plot above, from the left to the right.
Note: since the LED will never be operated with reverse DC bias (no light emitted), we don't model it.

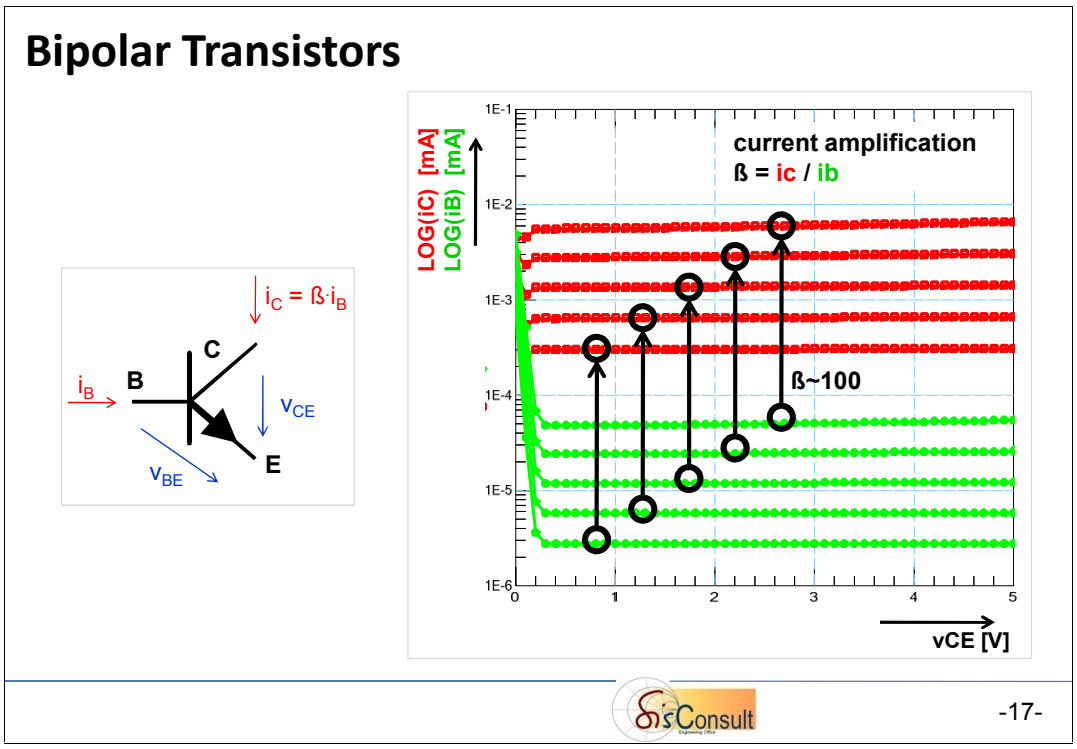
Developing the LED model:

- Diode 'D1' models the lowest forward DC bias up to ~2.1V.
  Its y-intercept is modeled by parameter D1.IS, and the slope by D1.N
- For DC biases above this range, D1 predicts a too low current 'i'.
  The additional current in this region is to be modeled by an additional current path, *in parallel* to 'D1'.
  And since the measurement result of this region is once again represented by a straight line, we apply again a diode: 'D2'. Its y-intercept is modeled by parameter D2.IS, and its slope by D2.N.
- Finally, the highest DC biasing range in the plot, with its declining curve:
  The simulated current 'i' prediction of diode 'D2' in this range is higher than what has been measured.
  Or, interpreted the other way, there is more measured voltage drop at the same current than what is simulated: we need to add a component in series.
  And so we add resistor 'RS', and for improved fit in the transient range, also a fitting diode 'D3'.
  (For the modeling experts: this is similar to the effect of the bipolar transistor Gummel-Poon model parameter IKF).

Note: It is interesting to note that the light emission of the LED takes place in this ohmic range. In the range of diode 'D2', the light emission is extremely small and practically not visible.

The netlist of the resulting WHilte LED model is finally (in SPICE syntax):

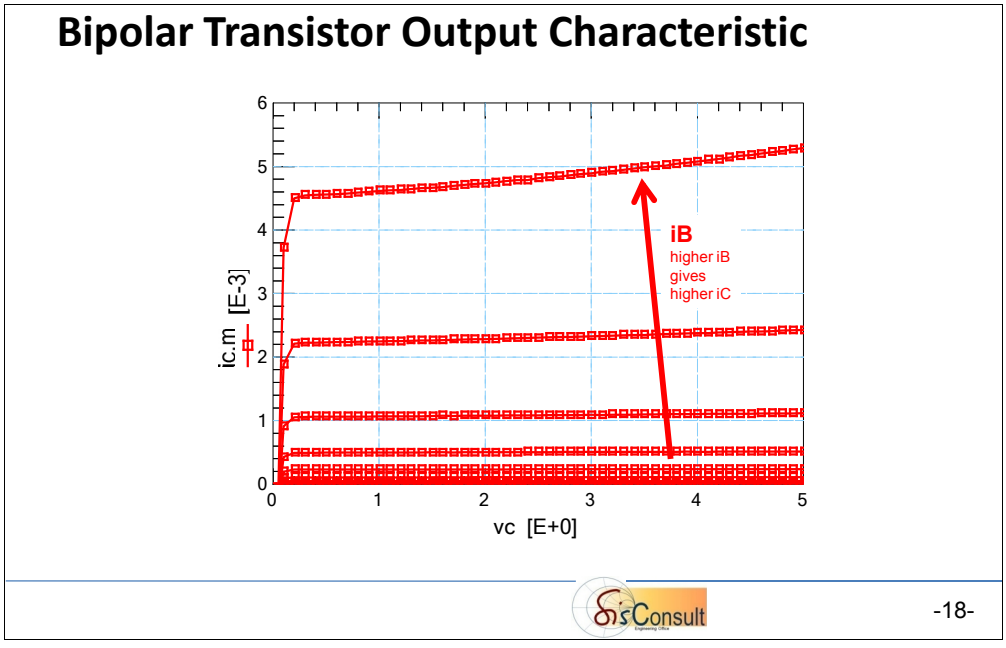
```
*    1=Anode (Plus)    2=Cathode(Minus)
.SUBCKT   LED_white    1  2

*model instances
RS          1   12  16.8
Dhigh      12  122  D3
Dmedium   122    2  D2
Dlow      122    2  D1

* model cards
.MODEL D1  D  IS = 6.87E-20  N = 3.12
.MODEL D2  D  IS = 4.57E-34  N = 1.42
.MODEL D3  D  IS = 0.00546   N = 4.69
.ENDS
```

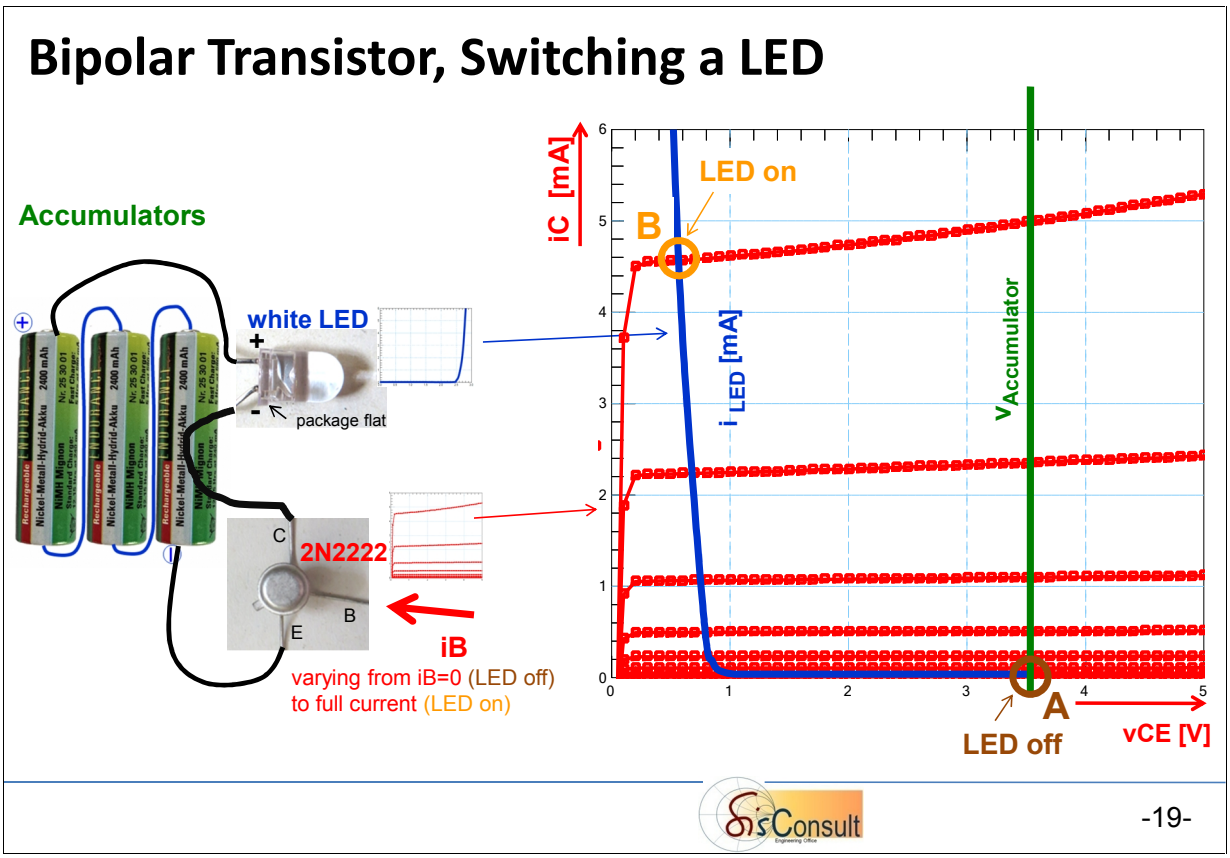


Simplified explanation of the functionality of a bipolar NPN transistor:
A current 'iB', flowing into the Base contact, is amplified to a much larger current 'iC', flowing into the Collector node. This is true under the condition that 'vCE' is larger than typically 0.5...0.7V.
In the example above, this amplification factor ß = iC/iB is roughly a factor of 100.

Notice: current 'iB' into the Base means a voltage drop across the pins of Base B and Emitter E, i.e. V_{BE}

With this in mind, the slide below shows the so-called transistor output characteristics, i.e. the Collector current 'iC', versus the Collector-Emitter voltage 'vCE', as a function of the control current iB into the Base contact.
Different to the previous slide, the iC-vCE measurement is now shown in a LIN/LIN scaled plot.
As discussed before, the Collector current 'iC' increases with increasing Base current 'iB':

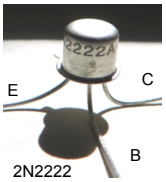


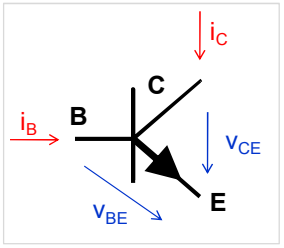


Considering the circuit shown on the left, and the measurement characteristics of each of its components plotted on the right,

- the maximum 'vCE' voltage for the transistor is the accumulator voltage '$v_{Accumulator}$' (green):
  $vCEmax=v_{Accumulator} \sim 3.6V$
- When iB=0, the whole circuit is in operation condition 'A', as indicated by the brown circle.
  The transistor's Collector current 'iC' is zero, and no current flows through the LED: no light is emitted.
- If the transistor Base Contact 'B' is fully powered, i.e. if the Base current 'iB' is at its maximum, 'iC' is also at its maximum, and the whole circuit is in operation condition 'B', visualized by the orange circle:
  'iC' flows through the LED, and this results in a voltage drop across the LED of ~3V.
  The transistor's resulting 'vCE' voltage is then
  $vCE = v_{Accumulator} - vLED \sim 3.6V - 3V = 0.6V$
- In other words: the two operation modes are a result of the overlay of the (red) transistor characteristic and the (blue) LED characteristic, together with the accumulator voltage (green).

Modeling the NPN Bipolar Transistor





Gummel-Poon model equations,
simplified for DC forward modeling

$$i_C = \frac{2 \cdot IS \cdot \exp\left(\frac{v_{BE}}{NF \cdot v_T}\right)}{1 + \sqrt{1 + 4 \cdot \frac{IS}{IKF} \cdot \exp\left(\frac{v_{BE}}{NF \cdot V_T}\right)}} * \left(1 + \frac{v_{CE}}{VAF}\right)$$

neglecting ohmic effects

$$i_B = \frac{i_c}{BF}$$

neglecting low iB current and ohmic effects

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The modeling of the bipolar NPN transistors is different from the so far discussed modeling procedures, because we can apply a specific, dedicated standard model. No need for sub-circuit modeling, what we had applied so far for the other components.
Standard models are developed and published for typical, widely used, standard devices, like our bipolar NPN transistor

The 2N2222 transistor used in our circuit is a NPN bipolar transistor. By the way, the bipolar transistor was the first semiconductor transistor, invented in the Bell Labs in the USA (1947) by J.Bardeen, W.Brattain and W.B.Shockley (honored by a Nobel Price in 1956). MOS transistors, the standard components in today's chips, were invented later.

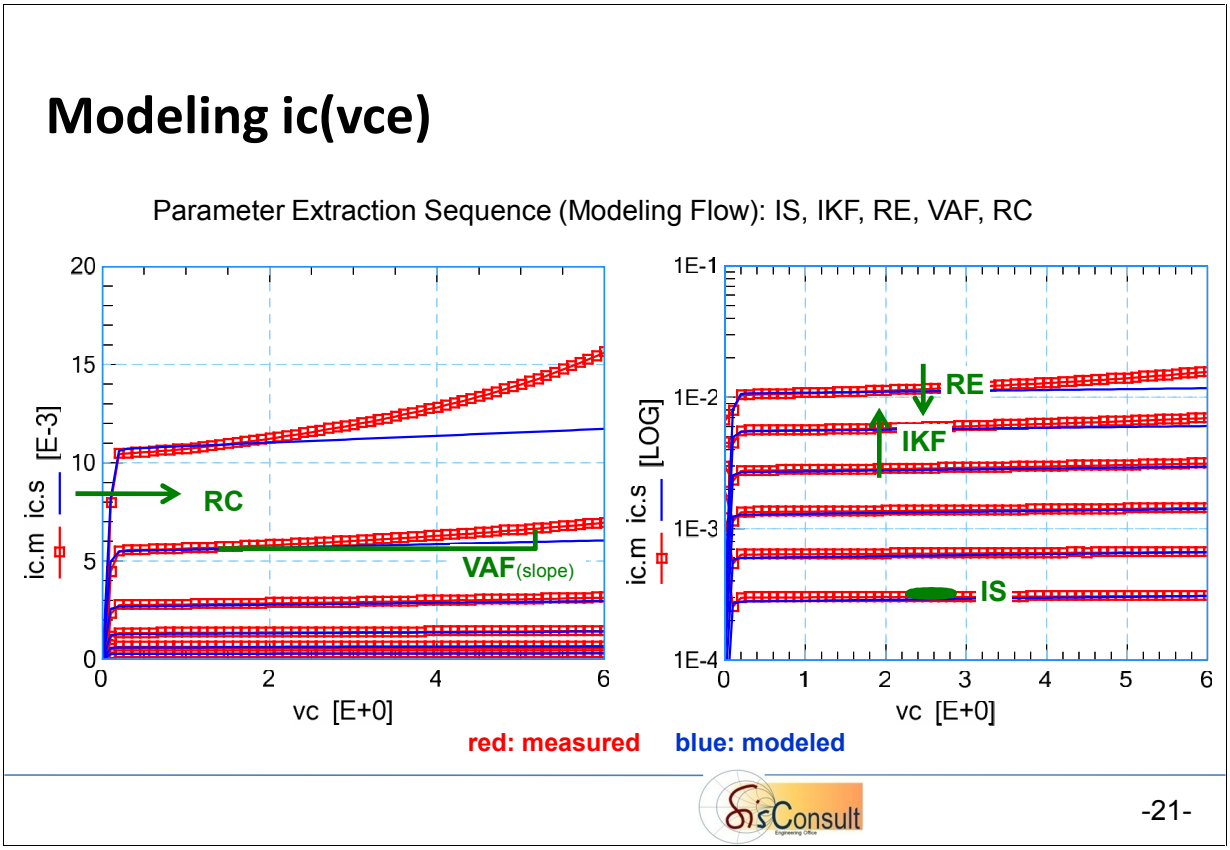
One of the standard models for this kind of transistor is the Gummel-Poon model (H.Gummel, H.C.Poon, Bell Labs, USA, 1970). Although more complex bipolar models are available now, it is still used until today. For our application, it is fully sufficient, and we will only consider the DC forward part of the model.

When applying standard models, it is important for the modeling engineer to inspect the model equations, and to identify measurement areas in which model parameters are dominant. The values of these model parameters can then be extracted from these areas.

Depicted in the slide above are the Gummel-Poon equations, for 'iC' and 'iB' and for DC modeling. They are simplified for our application, neglecting the losses across the transistor resistances at its Base, Collector and Emitter. Also, the ultra-low 'iB' range modeling (recombination range) is neglected.

The model parameters for this case are

```
IS    transport saturation current
NF    forward current emission coefficient (usually NF~1)
BF    ideal forward maximum beta
IKF   forward beta high current roll-off (transition to ohmic range)
VAF   forward Early voltage
```



As mentioned, when fitting a model to measurements, the modeling engineer first tries to identify the influence of model parameters to certain regions of the measurements. Another important knowledge of the modeling engineer is the sequence of parameter extraction, also called 'Modeling Flow'.

In the very much simplified Gummel-Poon modeling strategy for our 2N2222 transistor, the step-by-step procedure is:

Plot LOGiC(vCE):

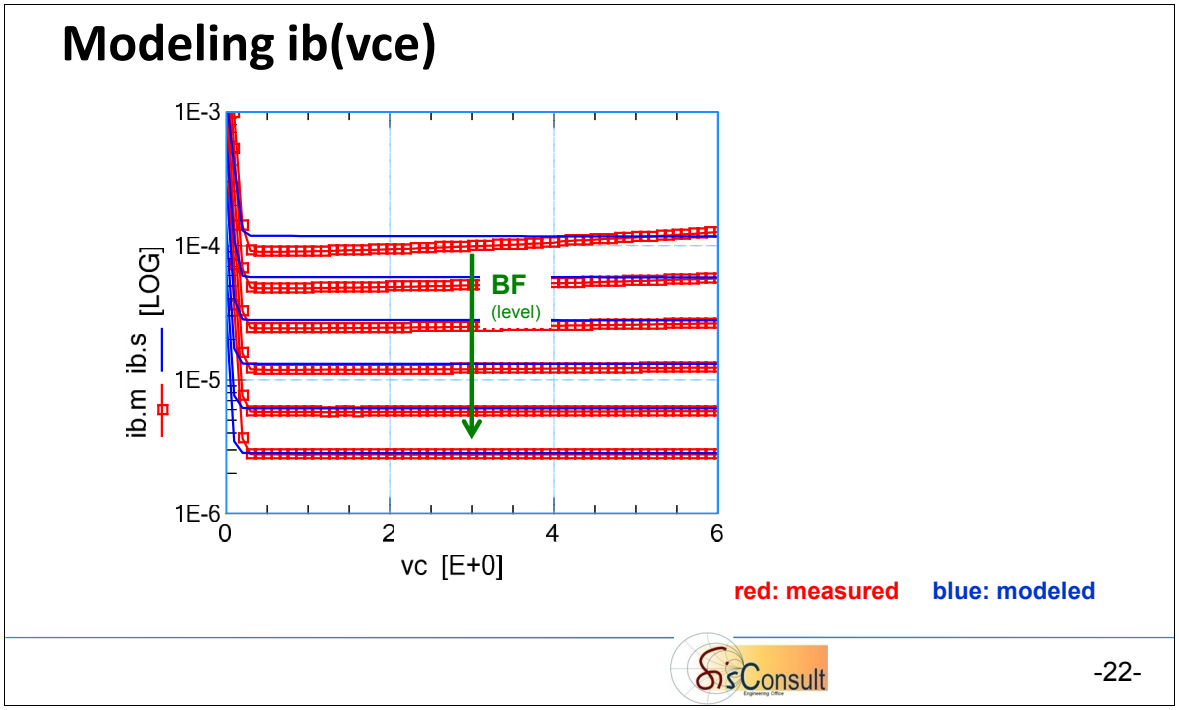
- IS: fit the lowest measured ic curve.
- IKF: fit the higher ic curves.
- RE: fit the highest ic curve.

Plot iC(vCE):

- VAF: match the slopes of the blue simulated curves (the model) to the measured red ones.
- RC: match the vCE<0.5V region

Note: in the linear Plot iC-vCE (above, on the left), the deviation for the highest curve, at high 'vCE', is related to the self-heating of the transistor. The classic Gummel-Poon model does not feature the modeling of this effect. Because this region is of no major interest for our application (no operation point for the transistor in our designed circuit), we can ignore it.

Once iC(vCE) is modeled, the input current iB needs to be fitted, as shown in the next slide:



To finish our modeling flow, we consider
Plot iB(vCE), once again in semi-logarithmic scaling:

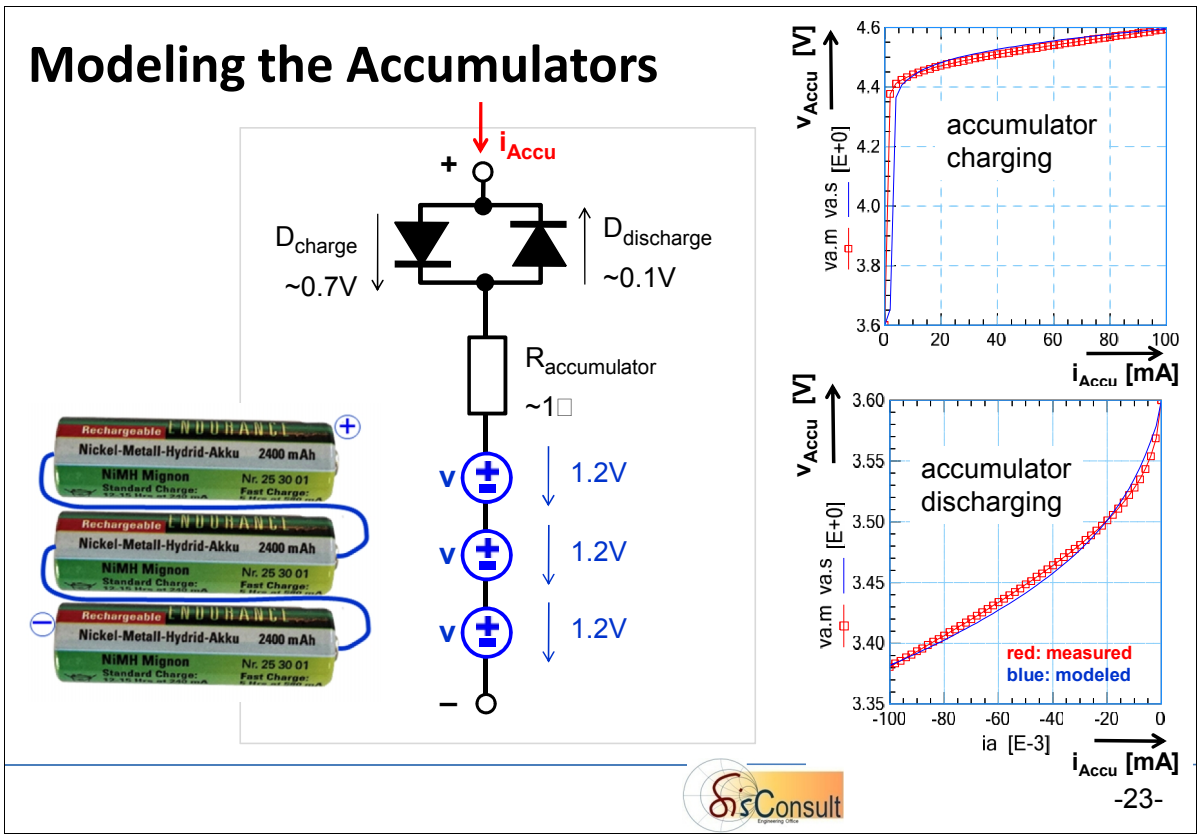
➢ BF: tune the value of model parameter BF to match the iB-curves.

Finally, the modeling netlist for the 2N2222 in forward DC operation is (in SPICE syntax):

```
*                       1=Collector   2=Base   3=Emitter
.SUBCKT   NPN_2N2222    1    2    3

* model instance
Q1   1   2   3   MAIN

*model card
.MODEL MAIN NPN IS   = 56.16f     NF   = 1.037
+               BF   = 109.5      IKF  = 130.1m
+               VAF  = 35.42      RE   = 0.12
+               RC   = 2.33

.ENDS
```

Notice:
if interested in a complete Gummel-Poon modeling example, see
'How to Model a BJT Bipolar Junction Transistor'

www.youtube.com/watch?v=UEqf0vDhlcw (Status Jan.2023)



For a simple, DC-only modeling of the accumulators, ignoring dynamic (time-dependent) effects, we apply a schematic as depicted above:

- the three Nickel Metal Hydride accumulator modules are represented each by a voltage source of 1.2V
- they are in series with a resistor '$R_{Accumulator}$'
- since the charging requires a roughly 0.7V higher voltage than what is delivered later during discharging, a diode 'Dcharge' with a voltage drop of ~0.7V is added. It is shorted during accumulator discharging by the diode 'Ddischarge', and its voltage drop of ~0.1V.

The netlist for the accumulator pack is (in SPICE syntax):

```
*                1=Plus      2=Minus
.SUBCKT  accumulator  1   2

*model instances
Dcharge        1     12   Dcharge
Ddischarge    12      1   Ddischarge
Raccumulator  12    122   394m
V1           122   1222   1.2
V2          1222  12222   1.2
V3         12222      2   1.2

*model card
.MODEL Dcharge     D1 D IS = 259.7p    N = 1.87
.MODEL Ddischarge  D2 D IS = 6.12m     N = 2.41

.ENDS
```

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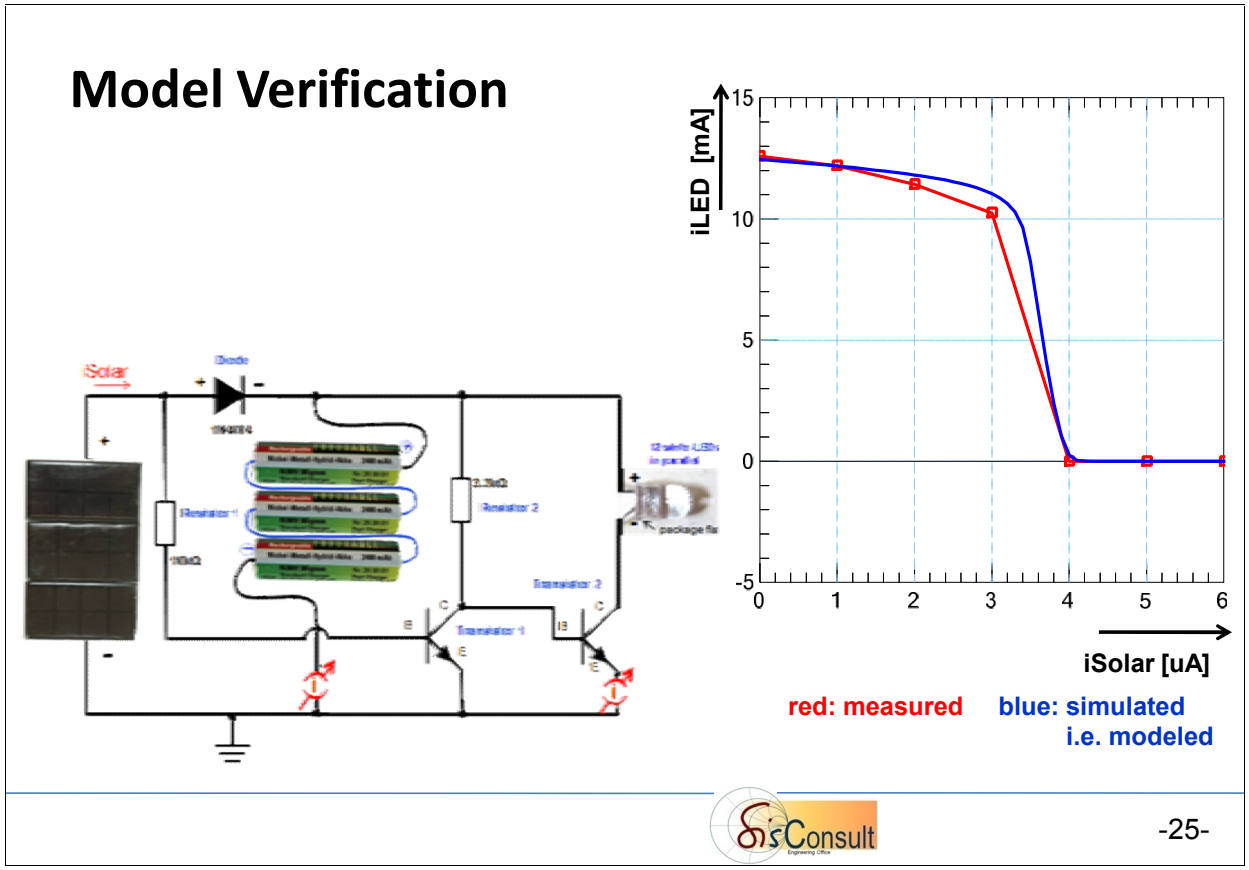
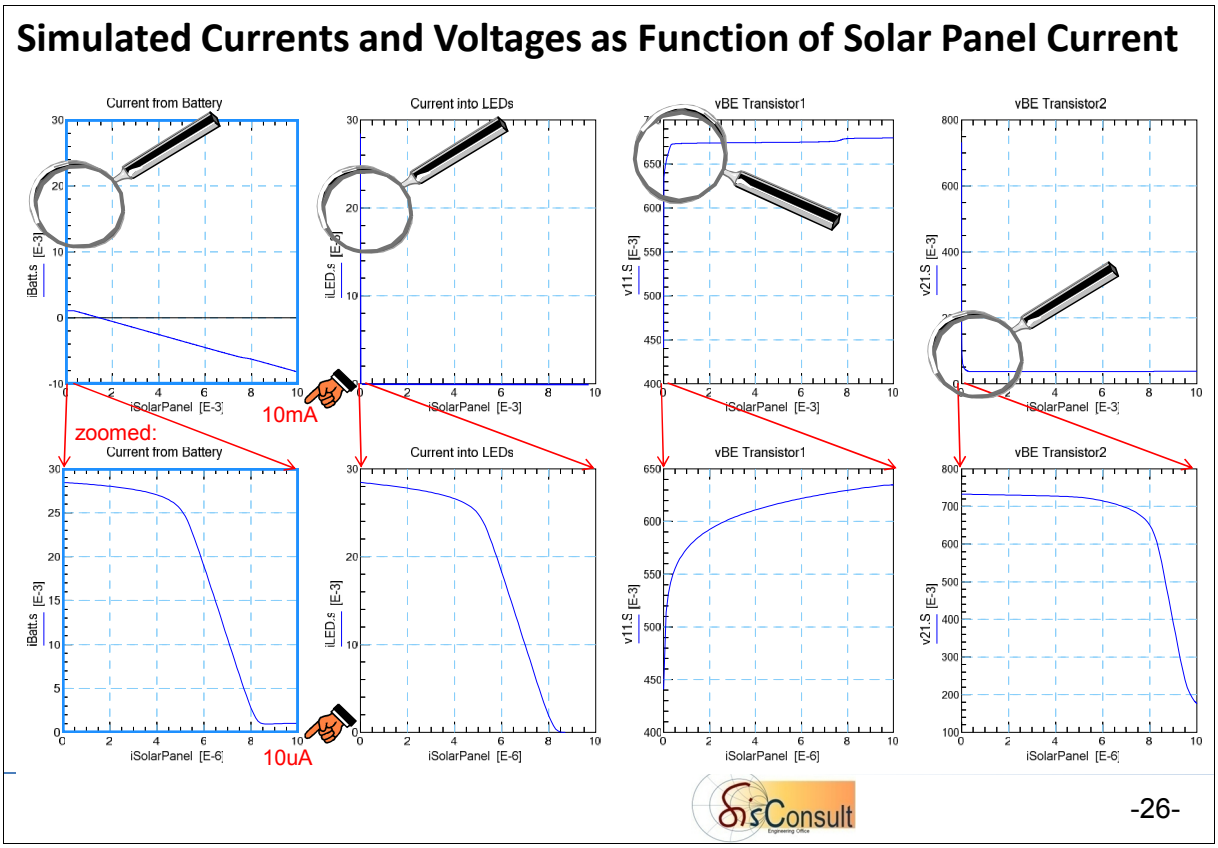
Verification of the Device Modeling

With all components of the circuit available as models, we now can simulate the whole circuit, and compare the result of this simulation with measurements.



For the measurement/simulation verification, depicted in the slide above, the solar panel has been replaced by a varying current source for both, measurement and simulation, sweeping from 0A (night time: LED is on) to 6uA (sun light: the LED is off, and the accumulators begin to being charged).

For completeness, here the simulations of the currents and node voltages for a solar current from 0A to 10mA (top row), and zoomed from 0A to 10uA (bottom row):



CONCLUSIONS:

Modeling Engineers provide models, i.e. mathematical formulas, to describe the properties of electrical components like resistors, capacitors, inductors, diodes and transistors, but also of connectors, cables, mounting boards etc.

This enables the **integrated circuits (IC) design engineer** to develop circuits according to the requirements defined by the system engineers, without having the *individual* electrical components available physically.

If the models cover the device performance accurately and for all application domains, **the chip, finally fabricated in a wafer fab**, will work correctly right the first time of production.

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